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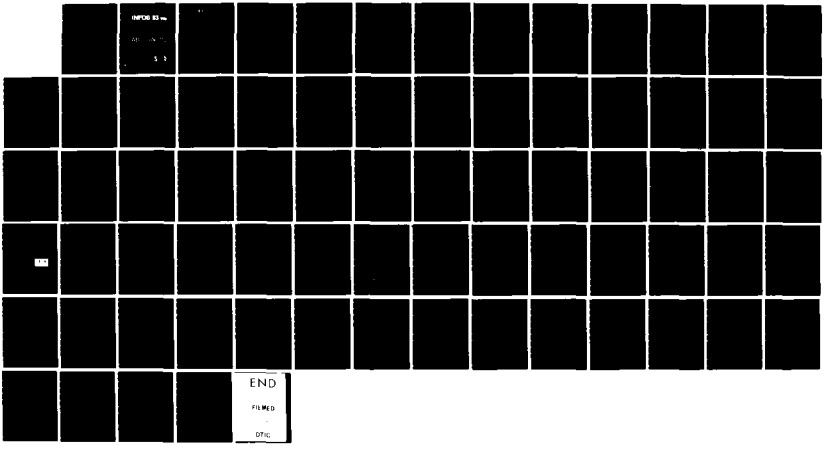

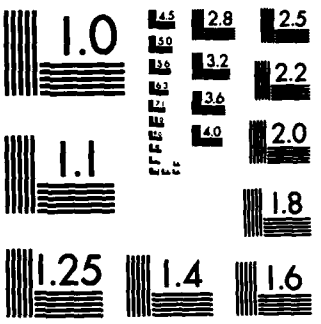

International Conference

INFOS 83

Insulating Films on Semiconductors

ABSTRACTS

11-13 April 1983
University of Technology
Eindhoven
The Netherlands

INFOS 83

Eindhoven
11-13 April 1983

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Model of Continuously Distributed Trap States at Si-SiO_2 Interfaces

Takuo Sugano

ABSTRACT

Trap states between the Si-SiO_2 interface have been attracting much attention because these states take an important role in controlling the threshold voltage V_{th}, transconductance, and flicker noise of MOSFETs. However, the chemical and physical origins of these states have not been fully understood, although some attempts were made to shed light on these problems. In particular, little has been known about the theoretical background of the fact that these interface trap states are continuously distributed in energy.

A calculation dealing with the electronic structures of crystalline Si-amorphous SiO_2 interface including microstructural defects has been carried out being based on semiempirical tight-binding Hamiltonians and Green's function formulation and applied to the calculation of interface trap states between amorphous SiO_2 and the Si substrate with (111) orientation.

The model was a crystalline Si with (111) orientation and amorphous SiO_2 represented by a Bethe-lattice. This can be considered as a Cluster-Bethe-lattice model and the cluster is the crystalline silicon, whose dangling bonds are terminated by the SiO_2 Bethe-lattices.

The following results were obtained. The perfect interface and the interface including oxygen dangling bonds have no energy level in the Si band gap, whereas the Si $\equiv$ Si- dangling bond has an energy level at about the middle of the Si band gap. Si-Si weak bond and weak interaction at the interface give rise to gap states whose energy move in the energy range lower than the midgap with varying the distances between two Si atoms as shown in Fig. 1, while the energy levels of Si-O weak bond and weak interaction at the interface appear at the upper half of the forbidden gap of Si depending on the distances between the Si atom and the O atom as shown in Fig. 2.

Possible origins of interface trap states which are distributed continuously in the Si energy gap as illustrated in Fig. 3, are suggested to be these Si-Si weak bonds, Si-Si weak interactions, Si-O weak bonds, and Si-O weak interactions, at the interface, whose bond lengths are distributed as illustrated in Fig. 4.

From these model, the interface traps in the lower half of Si bandgap are thought to be donor type and those in the upper half are to be acceptor type.

The reduction of the gap state density by H_2 annealing, trichrolo-ethylene annealing, or HCl oxidation is understood by bonding H or Cl to the Si $\equiv$ Si- dangling bond at the interface.

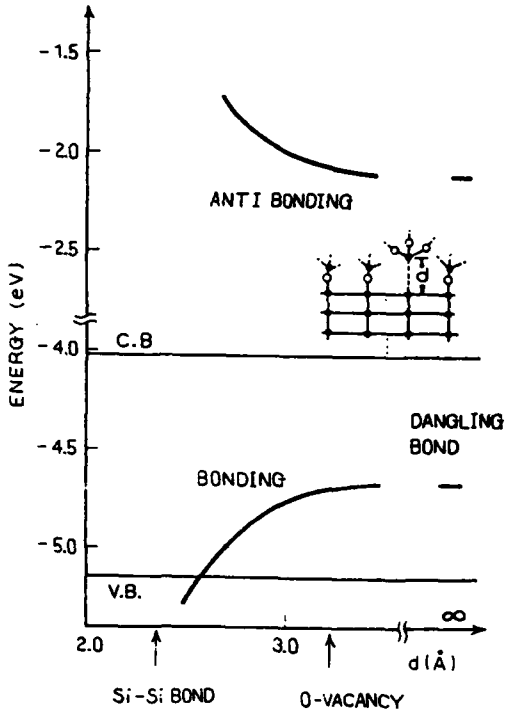

Fig.1. Si dangling bond, Si-Si bond, and O-vacancy level at the interface. These energy levels move in the lower half of the Si band gap with changing the bond length d. Open and closed circles denote O and Si atoms, respectively.

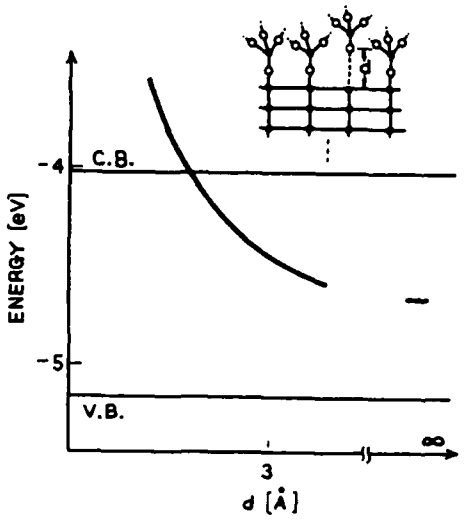

Fig.2. Energy level of Si-O weak bond at the interface. This energy level moves in the energy range higher than the midgap with changing the bond length d. Open and closed circles denote O and Si atoms, respectively.

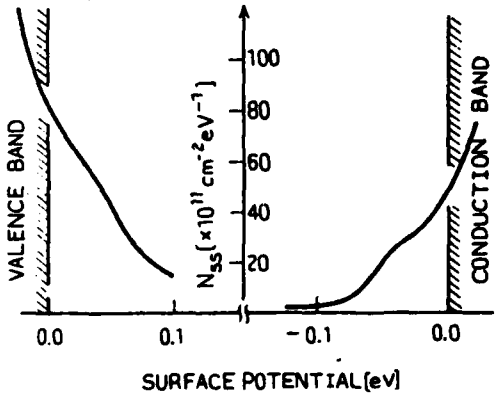

Fig.3. Commonly observed U-shaped distribution of interface trap-state density in the forbidden gap of Si.

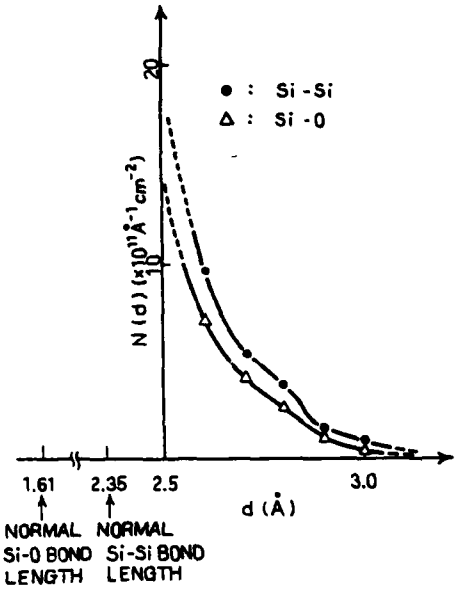

Fig.4. Assumed bond length density $N(d)$ ($Å^{-1}cm^{-2}$) vs bond length d (Å). Using this distribution together with the energy level dependence on bond length of Fig.1 and Fig.2, U-shaped distribution as shown in Fig.3 can be explained.

Gold Distribution Profiles in the $Si-SiO_2$ Interface Region

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Measurement of gold distribution profiles in MOS structures may be used to probe the reaction kinetics, e.g. the generation of interstitials and vacancies at the $Si-SiO_2$ interface during high temperature processing. The conversion of the fast diffusing interstitial gold into electrically active substitutional gold is proportional to the concentration of vacancies (Frank-Turnbull mechanism) or inversely proportional to the presence of interstitial silicon (Kick- Out mechanism).

The concentration profile of substitutional gold may be determined by the well-known trap levels associated with gold. In the experiment, we have implanted gold doses ranging from $10^{12}cm^{-2}$ to $3 \times 10^{13}cm^{-2}$ into the back of an oxidized p-type Si substrate. The Au-diffusion to the $Si-SiO_2$ interface was performed at temperatures from 900°C to 1100°C. Deep level transient spectroscopy (DLTS, CC-DLTS and DDLTS) was applied to MOS capacitor structures for the determination of interface state and bulk level spectra. For portion of the sample area, the front oxide was removed after Au-diffusion. In this case, Schottky diodes were fabricated for the depth profile measurement.

Besides the well-known gold level at $E_v+0.35$ eV two gold related levels at $E_v+0.45$ eV and $E_v+0.52$eV were observed. The concentration of all three levels are dependent on the gold dose implanted. The background interface state density is reduced after the Au diffusion. The substitutional gold concentration is constant or increases towards the interface. In a detailed discussion of the results observed, the generation of vacancies and/or interstitials during oxidation and its influence on the gold diffusion has to be taken into account.

ELECTRICAL CHARACTERIZATION AND MODELING OF FIELD-SENSITIVE INTERFACE STATES

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ABSTRACT

We have recently reported[1] on the generation of interface states in SiO_2 capacitors that are field- and time-dependent, as well as thermally activated. The states appear to be the result of neutral defects present at the interface that can be made electronically active by the application of an electric field. The amount of field-sensitive interface states is observed to be linearly dependent on the applied field for positive bias and displays a threshold field for introduction. A $t^{1/4}$ time dependence is also observed for the interface state generation. Recent measurements performed with negative bias display however a more complicated field as well as time dependence.

We have proposed a model of candidate defects whose physical and electronic properties are consistent with the effects observed in our experiments[2]. This model is derived from the Valence-Alternation-Pair (VAP) model proposed originally by Street and Mott for amorphous chalcogenides[3]. Our formulation of the model involves the basic stipulation that oppositely charged, over- and under-coordinated oxygen centers exist throughout the bulk of the oxide as well as at the interface itself in the form of near-neighbor pairs, i.e., Intimate-Valence-Alteration-Pairs, IVAP's. These states are distributed in energy in the oxide band gap so that a substantial fraction of localized levels are found in the silicon band gap with positive donor states located primarily in the upper half of the band gap and negative acceptor states in the lower half. The IVAP defect is then a neutral scattering center when the pair separation is approximately one inter-atomic distance. This would explain why it is not normally observed in C-V measurements. However, when an electric field of sufficient strength is applied to the oxide, a force is exerted on the defect separating its two charged members. The appropriately charged defect (as determined by the polarity of the field) can diffuse towards the interface by a mechanism consistent with the observed $t^{1/4}$ behavior. The defect member at the interface can then function as an interface state. The fact that the separated charged states have different properties can be used to provide an explanation for the observed asymmetry between positive and negative bias conditions. The model thus provides a natural microscopic framework for a bipolar defect which is also consistent with existing data on the buildup of interface states caused by charge injection or ionizing radiation. More recent experiments (now in progress) involve measurements of cross-sections for carrier capture under different bias conditions. The results so far further corroborate the bipolar nature of the defect. A modified model incorporating Silicon as well as oxygen -derived defects is also formulated and compared with other existing models for interface state generation.

REFERENCES:

(1) J.L. Crowley, T.J. Stultz and S.K. Ichiki, Appl. Phys. Lett. 38, 1012 (1981).

(2) J.L. Crowley, H.J. Hoffman and T.J. Stultz, J. Appl. Phys. 53, 6919 (1982).

(3) R.A. Street and N.F. Mott., Phys. Rev. Lett. 35, 1293 (1975).

Generation of interface states in MOS and MIOS structures by high field injection

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Due to its negative effect on device characteristics the generation of interface states upon carrier injection in the gate insulator of MOSFETs and nonvolatile storage devices with MIOS gate has been the subject of several recent studies /1/. We have made an investigation of the number of field injected charge carriers required for the generation of one interface trap (n_{inj}/N_{it}) in MOS, MNOS, MAOS and MANOS (O = SiO_2; N = Si_3N_4; A = Al_2O_3) capacitors at room temperature and liq. N_2 temperature. Further experimental variables were the thickness of the SiO_2 film and also the temperatures of oxidation and post-oxidation annealing in N_2.

The ration n_{inj}/N_{it} varies strongly for the different samples and depends on the sign of the gate voltage. In all cases the distribution of the interface states created by carrier injection extends over the entire band gap. An additional peak at approx. 0.7 eV above the valence band edge is always obtained except for MAOS and MANOS structures at positive gate voltages. From a knowledge of the carrier type in the insulator system and using our observation that upon injection of carriers by means of the avalanche technique the 0.7 eV peak only appears in the case of holes we will present model considerations related to the concepts proposed by Suzuki et al /2/ to explain our data.

/1/ P. Balk and N. Klein, Thin Solid Films, 89, 329 (1982)

/2/ E. Suzuki, Y. Hayashi and H. Yanai, J. Appl. Phys., 52, 6377 (1981)

PARAMAGNETIC DEFECTS IN OXIDIZED SILICON WAFERS COATED WITH LANGMUIR-BLODGETT FILMS

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and

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ABSTRACT

ESR experiments[1, 2] on silicon/silicon oxide structures have demonstrated a quantitative correlation between the amplitude of observed resonance signals and the density of mid-gap densities of states. However, attempts to investigate how a gate voltage might affect the population of the spin centre have not been entirely successful due to leakage currents. In this paper we report how this problem may be solved by overcoating the oxide with a few monolayers of various organic materials deposited using the Langmuir trough technique[3]. Results will be presented for the paramagnetic P_b centre ($\cdot Si \equiv Si_3$) at the Si/SiO_2 interface with a magnetic field applied perpendicular to the (111) surface.

The variation of the e.s.r. signal amplitude with applied gate bias has been studied as a function of the microwave power level for a 1000Å thick oxide layer structure. It is interesting to note that in the inversion region the amplitude is independent of e.s.r. power. This indicates a short relaxation time due to the coupling of P_b spins with mobile electrons attracted to the interface. On the other hand, in the accumulation region, where there is a majority of holes and therefore a longer relaxation time, the amplitude varies as $(\text{power})^{\frac{1}{2}}$ as predicted classically.

With oxides less than 100Å thick on Si wafers, different defects and properties occur. In this case the e.s.r. signal from the P_b defect centre can be reduced or eliminated by adsorption of highly electronegative or electropositive gases on the outer oxide surface, explained by extreme band bending and concurrent addition or removal of an electron from the P_b centre. Therefore, results will also be presented for MOS structures with a very thin oxide sealed by a Langmuir-Blodgett film.

1. P. J. Caplan and E. H. Poindexter, J. Appl. Phys. 50 5847 (1979).

2. E. H. Poindexter and P. J. Caplan, J. Appl. Phys. 52 879 (1981).

3. G. G. Roberts, Proc. Erlangen Conference on Insulating Films on Semiconductors (Springer-Verlag, 1981, ed. Schulz) p. 56.

CORRELATED ELECTRON PARAMAGNETIC DEFECTS AND DEEP LEVELS AT THE OXIDIZED SILICON SURFACE. E. H. Poindexter and P. J. Caplan, US Army Electronics Technology and Devices Laboratory, Fort Monmouth, NJ 07703; N. M. Johnson, D. K. Biegelsen, M. D. Moyer, and S. T. Chang, Xerox Palo Alto Research Center, 3333 Coyote Hill Road, Palo Alto, CA 94304.

Thermal oxidization introduces electrically active defects at the surface of single-crystal silicon. Two experimentally observed manifestations of these defects are: (1) a continuous distribution of deep levels in the silicon bandgap, and (2) electron paramagnetic centers. From both capacitance-voltage and deep-level spectroscopic measurements on as-oxidized silicon, the bandgap density of states at the surface is dominated by a broad peak centered approximately 0.3 eV above the valence-band maximum. Electron spin resonance (ESR) reveals a paramagnetic center at the interface which has been tentatively identified as a trivalent silicon defect bonded to three silicon atoms, with the dangling bond oriented normal to the surface on (111) silicon. These manifestations of interface defects display similar dependences on oxidation conditions and silicon crystal orientation. To establish directly the correlation between interface states and the spin center, both electrical and ESR measurements were performed on the same samples. For this purpose, large-area metal-oxide-silicon capacitors were fabricated which permit in situ electric-field modulation of the surface potential during ESR measurements. The spin density, measured with proper account taken for the electric-field dependence of the spin-lattice relaxation time, maintains a nearly constant value across most of the bandgap, but drops rapidly to near zero near the conduction band and to about 25% of maximum near the valence band. This variation of the spin density with Fermi level is consistent with an amphoteric model of the paramagnetic defect which has been proposed for silicon dangling bonds in hydrogenated amorphous silicon.

Low T ESR study of interface defect centers on thermally oxidized Si wafers and the influence of As^+ implantation.

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ESR measurements at 9.0 and 20.9 GHz have been carried out in the temperature range $4.2 \lesssim T \lesssim 40$ K and at RT on thermally-oxidized single-crystal boron-doped (100) Si wafers of various resistivities $\rho_{300\ K}$ = 0.24,20 and 50 Ω cm. Generally, two interface signals, both showing anisotropic g valu were observed and are identified with the Pb_0 and Pb_1 centers respective modelled by the $^{\circ}Si \equiv Si_3$ and $^{\circ}Si \equiv Si_2O$ unsaturated-bond models. Annealing in dry N_2 at 1050 °C does not change ΔB_{ptp} nor $g(\overline{B})$ except, maybe, for a slight overall increase in g-value of the Pb_0 signal. Intermediate-dose through-oxide (d_{SiO_2} = 104 - 130 nm) implantation of 10^{14} As^+ cm^{-2} at 60 or 80 keV makes both signals isotropic again, but subsequent N_2 annealing now restores the Pb_0 signal largely to its pre-implantation appearance, while this has no clear effect on Pb_1. Notwithstanding the satisfactory signal-to-noise ratio and the higher inherent resolution exhibited at K band compared to X band, the splitting up of the Pb_0 signal in only 2 components instead of 4, as predicted generally by the $^{\circ}Si \equiv Si_3$ model with an oblate almost axial-symmetrical g ellipsoid, could be observed. Computer-simulation assisted interpretation, fully incorporating linewidth observations, together with implantation and annealing results in addition with the X-band observations which reveal an important frequency dependency in ΔB_{ptp}, indicates the existance of a specific distribution of the $^{\circ}Si \equiv Si_3$ unsaturated-bond directions about the possible single-crystal interfacial directions; accordingly, improved g-tensor values have been deduced. This explains the differences observed over various sample sets reported before and shows these measurements to be apt to relate interface configurational 'quality' to the specific sample-preparation technique.

STATE OF THE ART IN InP MIS TECHNOLOGY

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Challenge between GaAs and InP to develop MIS structure on III.V. compounds has turned out rapidly in favour of InP. The behaviour of oxygen uptake on clean surface of both materials gives a real shortcomings to GaAs. As primarly shown by Spicer's works, excited oxygen is adsorbed by the GaAs surface, mechanism which increases the broken bonds at the semiconductor surface and contributes to the density of surface states. On the other hand, excited oxygen is just chemisorbed at the InP surface without breaking bonds, minimizing the surface states. Another factor, which makes InP more suitable to get an inversion layer through the gate field is the proximity of the conduction band of the levels formed by the oxygen (or by the metal) adatoms at the surface. In the opposite, defect levels created in GaAs are rather deep and pin the Fermi level near midgap, preventing to invert the surface of the corresponding MIS structure.

This explains the lot of efforts during the last ten years directed to the InP MIS technology after the unsuccessful attemps on GaAs.

Two main ways in the realization of the insulating layer could be used : one, oriented to a native oxide growth on InP, keeping in mind the good interfacial properties of thermal grown oxide on silicon ; the second, consisting in the deposition of a layer, like Al_2O_3 or SiO_2, presenting intrinsic excellent dielectric properties. Our purpose in this paper is to point out the salient features of these approaches.

The thermal oxidation of InP for MOS application needs lower temperature than 350°C to minimize the degradation of the substrate. Bulk oxide contains a low concentration of P-oxide, $InPO_4$ or P_2O_5 some controverse still existing on this nature, and a higher concentration of In_2O_3. Excess phosphorus appears at the interface under an elementary form when oxidation runs in dry O_2, and under a phosphate form, in wet O_2. For very thin oxides, $InPO_4$ rather than elemental P is present at the interface. As under 350°C, the growth rate is very low, the oxide layer (~100 Å) is often covered by a thicker deposited insulator like CVD Al_2O_3. Good stabilities of the drain current MISFET characteristics along time have been reported, but prohibitive surface state densities have been noticed, whose effect is a decrease of the electron inversion effective mobility.

The thermal energy has been also fully replaced or partially assisted by plasma, without a pronounced change in the oxide and interface composition ; the plasma grown oxide resistivity, still low, moves from 10^7 to $6\times10^9\,\Omega$.cm.

Among the anodic oxides, the KOH-grown, tartaric acide-grown and acid-glycol-water-grown are most often investigated. A non aqueous electrolyte using ammonium pentoborate in ethylene glycol buffered to a ph of 6 has been also reported, demonstrating that semiconductor treatment could prevent the formation of Fermi level pinning centers allowing inversion on n-type material. As a matter of fact, the electrolyte and growth conditions affects strongly the properties of the oxide and of the interface ; the oxidation is normally conducted at room temperature, in a high electric field, and growth rate is faster than

in thermal oxidation. In_2O_3 and P_2O_5 appear both in high concentration in the bulk oxide ; at the interface, P_2O_5 is found instead of elemental P in thermal oxide, providing a gradual transition between the anodic oxide and the InP substrate. The oxide resistivity, limited to $10^{12}\Omega$-cm, is increased to $10^{15}\Omega$cm when using an electrolyte (HPO_4 with propylene glycol) of pH < 2.5 which dissolves out In_2O_3 in the growing oxide, as P_2O_5 presents a larger bandgap (6_10eV) than In_2O_3 (3.1 - 3.7 eV). The lack of reliability and reproducibility is certainly the problem to overcome with anodic oxides on InP.

Plasma anodization techniques have been likewise developed on aluminium films deposited on the InP substrate to obtain an Al_2O_3 - InP structure - The inversion of just anodized n-type structure has been demonstrated ; for thicker oxides, the increase of the trap centers at the surface occurs ; the reduction of the anomalous hysteresis of the C-V plots of MIS diodes is achieved by annealing in Argon at 250°C. A good resistivity ($10^{14}\Omega$-cm) and high breakdown fields ($4x10^6 V\ cm^{-1}$) are commonly reported. Low surface states densities evaluated to $4\text{-}7x10^{11}\ cm^{-2}eV^{-1}$ have allowed the fabrication of Mesa and Planar type MISFET on Fe doped S.I. InP with effective electron channel mobilities up to 2500 cm^2/vsec. and stable DC operation.

InP-oxide films have finally been produced by sputtering an InP target in an oxygen DC excited plasma, leading to equal proportion of In and P oxidized, and no accumulation of P at the interface. Resistivity of the layer : $3x10^{12}\Omega$-cm ; breakdown field : $1{,}5x10^5$ V/cm. Further work on this process is needed at the moment to avoid the C(V) characteristics dispersion.

If now the insulator film is deposited, SiO_2, Al_2O_3 and Si_3N_4 are most widely used. As a general statement, the layers exhibit high resistivities (> $10^{15}\Omega$-cm) and breakdown fields higher than $1x10^6\ V.cm^{-1}$, whatever the deposition technique is. That means dielectric properties are no longer a critical factor of the process. Conversely, low surface state densities and elimination of instabilities in the behaviour of the MISFET become the first objectives to reach.

Deposition of Al_2O_3 by sputtering uses a similar equipment as in the preceeding section, with an Al instead of InP-target. This technique does not seem to be much studied, much less than the electron beam Al_2O_3 evaporated from a sapphire target in oxygen atmosphere at 10^{-5} torr on InP. A surface state density lowered to 10^{11} states $cm^{-2}\ eV^{-1}$ is obtained by an annealing procedure, but a significant hysteresis of the C(V) curves attributed to trap centers in the first layers of oxide should be reduced.

The Chemical Vapor Deposition could appear as the most versatile method according to the various options proposed by this technique. SiO_2 or Si_3N_4 are generally obtained by pyrolysis of silane reacting with O_2 or NH_3. As already noticed, the temperature should not exceed 350°C. Used just as it is, this procedure has been applied successfully to realize a self aligned process for InP MISFET. The gate film is SiO_xN_y whose dielectric constant lies around 3.3 ; electron channel effective mobility is 1000 $cm^2V^{-1}\ sec^{-1}$. However a source to drain leakage current is present at zero gate voltage. Improvement of these results is achieved by a prior HCl etch in-situ ; are observed : a zero flat band voltage, a reduction of surface states close to the conduction band allowing the structure to accumulate, a small hysteresis (0,1V, for 1200 Å - SiO_2 layer).

Another evolution of the process consists in using partially the kinetic energy of electrons delivered by a plasma to activate the reaction ; this is the plasma-enhanced CVD. The best results on channel mobilities and transconductance of MISFET are obtained with Al_2O_3 and with SiO_2 (2100 and 220 cm^2/V.sec ; 63 and 15 mS respectively). Surface channel CCD have been also fabricated. Estimation of the trap state densities with time constant between 1 and 10^{-7} sec. could be as low as $5x10^{-9}\ cm^{-2}$; but, when traps exist, they are very slow.

If PECVD could be the most attractive way to produce MIS structures on InP, attention is now focused on the role that should played the thin native oxide preserved on the InP surface prior to the dielectric deposition ; its preparation, composition and stability could be determinative to optimize its interface properties (120 Refs).

CHLORINE INCORPORATION AND THIRD PHASE DEVELOPMENT AT THE Si/SiO_2 INTERFACE DURING THE OXIDATION OF SILICON IN $HCl-O_2$ AMBIENTS

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Total Cl content and Cl concentration versus depth profiles have been determined for a range of oxidation conditions by nuclear backscattering and SIMS. Oxidation conditions varied in the range: T = 1100-1200°C, HCl = 1-13%, time = 10-120 min. In several sequences the HCl was derived from trichloroethane. Si/SiO_2 interfacial morphology was determined by electron microscopy (TEM and STEM). X-ray microanalysis was used to determine Cl lateral segregation along the interface (in STEM mode). For Cl content $\lesssim 2\times10^{15}/cm^2$ no third phase was seen in TEM and no lateral nonuniformity of Cl concentration could be detected. Cl concentration profiles increase smoothly from $10^{17}/cm^3$ near the gas/SiO_2 interface to a peak near the Si/SiO_2 interface with Cl value in the range $4\rightarrow10\times10^{20}/cm^3$. For Cl content in the range $2\rightarrow4\times10^{15}/cm^2$ individual particles of a Cl-rich, amorphous phase develop at the Si/SiO_2 interface. The particles appear circular when viewed normal to the interface. The particles are less than 5 nm thick with an average diameter of 20-40 nm. Cl content of this phase is 2→4 times that of the matrix which still contains $\sim2\times10^{15}$ Cl/cm^2. The particles are nearly uniformly distributed at higher temperatures and become more clustered at lower temperatures. Results of quantitative metallography will be presented. The Cl profiles through the oxide are similar to those described above but the interfacial peak is higher. Oxygen concentration profiles still exhibit a very sharp drop (<5 nm) at the interface. Hydrogen concentration profiles are also very high in the bulk oxide with a peak at the interface. For total Cl > $3\rightarrow4\times10^{15}/cm^2$ clustering and agglomeration of the third phase particles becomes the dominate feature of the microstructure. Fewer, larger (~1 μm) particles are seen and Cl analysis indicates thickening of these particles. Preparation sequences with independently varied Cl_2 and HCl partial pressures (by H_2O addition) show Cl_2 to control the Cl incorporation process. Models will be suggested for Cl incorporation and third phase development.

Influence of annealing temperature on the mobile ion concentration in MOS structures

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Thermally grown oxides (1000° C, dry O_2) on monocrystalline Si (100, n-type, 2 - 5 Ωcm) have been annealed in a dry N_2 atmosphere at temperatures in the range 500° - 1000° C. The mobile sodium concentration N_m was determined after Al-electrode E-gun evaporation from triangular voltage sweep measurements (TVS).
A maximum for the value of N_m was found at annealing temperatures in the range 600° - 800° C (see the figure).
We investigated the influence of some other parameters of the anneal, particularly the duration, the ambient and the effect of a second anneal at a different temperature. A significant result was that the final anneal before the metallization appeared to be decisive for the level of sodium contamination.
A tentative explanation for the maximum of N_m as a function of the annealing temperature will be given.
Also the TVS results of thermal anneal applied to Na^+ ion-implanted oxides will be presented.

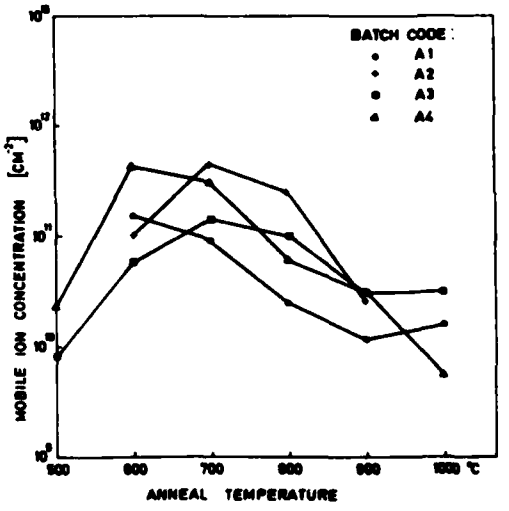

Figure: N_m as a function of T_{ann}, measured with TVS at 300° C on four consecutive batches.

Diffusion of Ion Implanted Ga, In and Tl in SiO_2

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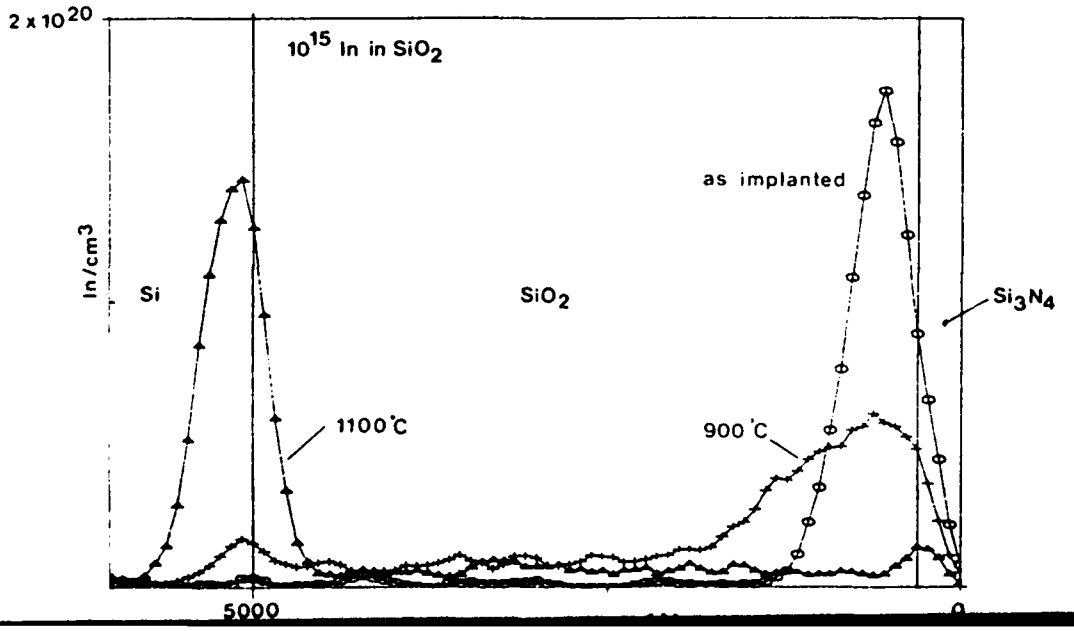
Gallium, indium and thallium were implanted into thermal SiO_2 grown on ⟨100⟩ silicon wafers, with fluences of $1x10^{15}$ cm^{-2} and $1x10^{16}$ cm^{-2}. After this the wafers were annealed at temperatures between 800°C and 1200°C in flowing N_2 gas. The resulting concentration profiles were measured by means of Rutherford Backscattering Spectrometry.
For Ga and In hardly any diffusion towards the SiO_2-Si interfaces was observed after annealing upto 1200°C. In contrast to these results Tl diffused rapidly into the oxide at 800°C. In all cases evaporation from the SiO_2 was observed, which was very strong in the case of Tl implants. Therefore a second set of experiments was set up in which we covered the SiO_2 with a LPCVD-Si_3N_4 layer before implantation. In these experiments we observed significant diffusion of Ga, In and Tl at 800°C towards the SiO_2-Si interface. From the concentration profiles it turned out that in all cases two diffusion mechanisms were present. One of the most remarkable features of these experiments was the observation of enormous segregation of In and Tl at the SiO_2-Si interface. In the figure below we show the concentration profiles of indium for various annealing temperatures to illustrate this effect. The gallium implanted samples did not show this segregation but in this case diffusion into the underlying silicon was observed.
The results of both types of experiments will be discussed in terms of the chemical nature of Ga, In and Tl in SiO_2.



ENHANCED GROWTH OF OXIDE LAYERS ON Si USING LASER RADIATION

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ABSTRACT

We report the use of continuous Argon-ion and CO_2 lasers to prepare oxide layers on the surface of Si. By preheating the samples to 300-400°C, and exposing them to either 500 nm, or 10.6 μm radiation, oxide layers thicker than 2000 Å have been grown. These are shown to have a refractive index n = 1.465 ± 0.01 for thicknesses 400-1400 Å, and consist of SiO_2 as indicated by the appearance of a strong 1070 cm^{-1} band in the IR spectra which is due to Si-O band stretching.

Evidence is presented for an enhanced oxidation rate when bandgap radiation is used to locally heat the Si lattice. This is most apparent in the 850-1050°C temperature range, and is thought to be due to the increased carrier population in the conduction band resulting from the absorption of Argon laser radiation. A model relating the density of antibonding states to the rate of oxidation is shown to qualitatively agree with experimental evidence, and underlines the importance of photo-induced effects in addition to the normal thermal mechanisms. This further implies the significance of the actual density of broken Si-Si bonds in the Si oxidation reaction in this temperature range.

MOLECULAR BEAM EPITAXIAL GROWTH OF CaF_2 and $Ca_x Sr_{1-x} F_2$ on GaAs

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Group II fluorides are known to be good insulators. Since their structure is closely related to the zinc-blende structure, lattice matching to III-V semiconductors can be obtained using mixed fluorides. This can be achieved by molecular beam epitaxy (MBE) Since the fluorides should transport by sublimation as undissociated molecular units.

Epitaxial growth of BaF_2 films on InP and CdT_e, and of CaF_2 on Si has already been reported. Here, MBE of CaF_2 on GaAs and of lattice matched $Ca_xSr_{1-x}F_2$ on GaAs is reported for the first time to our knowledge.

In our experiments, layer deposition was carried out in a vacuum chamber equipped with ion pumping. The evaporation cell was made with graphite and tantalum, and for a cell temperature of 1260°C, the growth rate was about 1000 Å/h. Layers 1000-2000 Å thick were deposited on (100) and (110) GaAs substrates mounted on a heated molybdenum block. Prior to loading in the vacuum chamber, the substrates were chemically etched and, once under vacuum, the temperature was raised up to 600°C in order to eliminate the thin oxide layer on the GaAs surface.

The epitaxial conditions were first studied for CaF_2/GaAs. For substrate temperatures higher than 300°C, the deposited layers were expitaxial, with the same crystallographic orientation as the substrate, i.e.(100) or (110). On the transmission electron diffraction (TEM) patterns, spot splitting was observed due to the lattice mismatch between layer and substrate.

For $Ca_x Sr_{1-x} F_2$, substrate temperatures above 300°C also led to epitaxia growth. The surface morphology of the fluoride layer did not show any particular feature and the aspect was smooth and mirror like. TEM diffraction patterns show no noticeable spot splitting, confirming that the mole fraction in the deposit is the same as in the evaporation charge and that, as expected, lattice match was obtained.

The uniformity of the composition and the interdiffusion between layer and substrate were studied using ion microprobe.

The dielectric and interface properties were investigated on MIS diodes made from $Ca_xSr_{1-x} F_2$ grown on GaAs.

Our results show that epitaxial fluoride layers, lattice matched to GaAs, with good insulator quality, are achievable by MBE, and this appears of great interest for use in MIS structures on GaAs.

Time Dependent Response of Interface States in InP MIS Capacitors Investigated with CC-DLTS Techniques

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Abstract

It will be reported for the first time on CC-DLTS measurements performed at InP-SiO_2 - MIS capacitors. Two types of samples have been investigated, one of epi - InP with $n = 1.4*10^{15}$ cm^{-3} and covered with an "undoped" SiO_2 insulating layer, sample A, the other of bulk material with $n = 10^{16}$ cm^{-3} and covered with an HCl-"doped" SiO_2 dielectric, sample B. For the explanation of the comprehensive experimental results a model will be proposed based on the assumption of a spatial and energetical distribution of interface states within the dielectric. The interaction of these traps with the conduction band takes place via a tunnelling process during the capture of electrons and by a tunnelling followed by a thermally activated transition during the emission process. The interface state density has been found to be about 10^{12} cm^{-2} eV^{-1} in the energy range between about 0.2 eV and 0.5 eV below the conduction band and to decrease considerably to the conduction band above about 0.2 eV. Thus accumulation can be reached. The interface state density strongly increases below about 0.6 eV at sample A and about 0.7 eV at sample B. Thus strong inversion could not been observed. It will be shown that the models presented previously are inconsistent with our experimental results while by the model proposed in the present paper most of the experimental results given in literature can be explained. Furthermore the results will be compared with those obtained at GaAs and silicon samples.

INFLUENCE OF NATIVE OXIDE ON SiO_2 - S.I. InP INTERFACE

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MIS structure properties can be improved if a good native oxide thin film is properly grown before dielectric deposition. Two different cleaning procedures have been applied to two samples of Fe doped semi-insulating InP before MIS process : one, using a $NH_4OH/H_2O_2/H_2O$ solution for 20 mn at 80°c named B3 by CNET, leaving a 20 Å $InPO_4$ native oxide (1) ; the other, the well known RCA procedure called HLH where a $HCl/H_2O_2/H_2O$ bath for 20 mn at 80° C etch the native oxide (2). Then on both substrates, the process consists of a 30 mn oxydation process assisted by plasma followed by a 1300Å thick layer SiO_2 deposition through plasma enhanced CVD specially designed for a homogeneous deposition. ϕ 375 µm Al dots are finally evaporated upon to realise the MIS capacitors.

The difficulty of the characterization is to eliminate the high resistivity (10^8 Ω.cm) effect of the S.I. substrate. This is achieved by using the phase-shift impedance technique (3) over a wide range of frequency (1Hz-1MHz). The main results are : evidence of accumulation and inversion is shown on both structures. Hysteresis indicating trapping effect move from 800mV tou 400mV on the sample with native oxide at 10KHz and vanishes at 11 Hz dealing with a large time constant of the traps. Interface states evaluated either by Therman's method using idealC(V) curves where the degenerescence effect in accumulation and inversion is accounted for, or the quasi state technique, give also the advantage to the native oxide. Composition of the insulator layer is analysed by a IR absorption spectrophotometer NIC 1180E showing the presence of effective SiO_2 much more porous than SiO_2 thermally grown oxide on Si but presenting very good insulator propecties.

REF. : (1) A. GUIVARC'H, H. LARIDON, G. PELOUS
Workshop on dielectric Systems of the III-V compounds SAN DIEGO, June 1982

(2) W. KERN, DA. PUOTINEN RCA Review, 31, 187 (1970)

(3) J. BOUCHER, M. LESCURE, M. MIKHAIL, J. SIMONNE - Relangen, RFA, INFOS 81 (1981)

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Characterization of Oxide Layers on $Hg_{1-x}Cd_xTe$ (CMT) and MCT-based IR Detectors by Combined Depth Profiling, SIMS, AES and XPS

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Previous characterizations of oxide layers on MCT /1/ have been extended by establishing surface analytical signature data for a great number of relevant Hg, Cd, and Te compounds. Thus, the nature of compounds and their depth distribution in native oxides on MCT, could be determined.
Based upon the analytical facility, several specific problems of MCT surface technology and IR device technology could be solved:

- Heating of native oxide layers under uhv conditions preserves the interface structure of Te and Cd, whereas mercury outdiffusion and oxygen penetration into the MCT substrate are observed. This fact may be responsible for the possibility of creating p-n-junctions in passivated MCT by heating /2/.
- Native oxide layers, which have been produced by various galvanostatic growth conditions (with or without removal of bulk material at the beginning of oxidations) do not differ from each other with respect to oxide composition. Differences are, however, observed concerning the nature and amount of impurities within the interface region, which might be responsible for the different electrical properties of the layers /3/.
- The depth profiles of photochemically grown native oxides reveal mercury outdiffusion and simultaneous Hg/Cd interdiffusion. The oxide-matrix interface width is larger than for electrochemically grown oxides and depends on the oxide layer thickness.
- The depth profiles of MCT based infrared detectors with native oxide passivation layers and ZnS antireflection coatings could be analyzed in view of the above results.

/1/ A. Benninghoven et al., in Proc. Infos 81 (eds.: M. Schulz, G. Pensl) Springer Series in Electrophysics, Vol. 7, Springer, Berlin 1981

/2/ M. D. Jenner, M. V. Blackman, British Patent No. 1600599 (1981)

/3/ B. K. Janousek, R. C. Carscallen, J. Appl. Phys. 53 (1982) 1720

Charge trapping in SiO_2

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Thermal SiO_2 is an insulator of key importance in silicon device technology, e.g. when used as the gate material in MOSFET's or in EAROM memory devices. As a perfect insulator it is expected to exhibit no physical defects, no fixed charges or interface traps and, moreover, to preserve these qualities even when the device is operating at extremely high electric fields.

Although during recent years immense efforts have been put into improving the yield and reliability of thin SiO_2-layers, it became clear that their properties depend on the details of the oxidation conditions, on the post-oxidation processing and on the electrode materials.
Aside from macroscopic imperfections, the SiO_2-layer may contain impurity-related as well as structure-related defects which will create energy levels in the insulator band gap. Impurities are usually introduced during processing, whereas the device may accumulate structural defects either during processing or under operating conditions (e.g. from radiation).

The defect-related energy levels will immobilize charge carriers whenever they penetrate into the insulator. In some cases the carrier trapping was used beneficially, e.g. to reduce electron leakage currents and improve breakdown characteristics, or in order to improve radiation hardness by attempting to balance electron and hole trapping. Mostly, however, the shift in device characteristics resulting from carrier trapping leads to an accelerated failure and should be avoided. Therefore, both the phenomenology and the kinetics of charge trapping should be studied carefully.

The sensitivity of the MOS-device to charges in the insulator makes it an ideal tool to study these phenomena. It became clear from studies concerned with ionizing radiation, however, that many insulator defects are initially present in an uncharged state and require electron or hole injection in order to become detectable.

After a description of the various techniques for carrier injection, charge location and trap analysis using MOS-structures, several examples of process-related charge trapping will be given. Both electron and hole trapping in SiO_2 induced by ion implantation, electron beam irradiation, and water incorporation will be discussed.

Many of these studies are concerned with bulk SiO_2 trapping, but information on the $Si-SiO_2$ interface can also be extracted. This becomes of vital importance when investigating e.g. radiation hardness of MOSFET's and, more recently, also interface degradation in VLSI devices. Injection of hot carriers into the oxide leads to interface trap and charge build-up which may be related to bulk SiO_2 phenomena although the available models are not unanimous.

In spite of its unsurpassed sensitivity for insulator charges, the MOS-device allows only an indirect identification of defect centers. In order to obtain more structural information on the $Si-SiO_2$ system other analytical techniques, such as IR-absorption and ESR, have been used recently and will be reported on briefly.

Hot Carrier Injection and Charge Trapping in N- and P-Channel MOSFETs

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Recently some controversy has arisen about the nature of the degradation effects (Q_{OT} and Q_{IT} generation) commonly associated with the injection and trapping of hot electrons in the gate oxide of small size n-channel MOSFETs /1/. Hot hole emission /2/ or the lateral drift of ions /3/ have also been invoked to explain the observations. To gain insight into the prevailing degradation processes we have compared the behaviour of n- and p-MOSFETs.

Before and after the drain voltage (V_D) stress experiments the gate-, substrate-, and drain (subthreshold) current vs. V_G were measured. For a given V_D the dependency of the degradation, e.g. the change of V_T or transconductance, on V_G was studied. Under normal stress conditions in the saturation ($|V_D| > |V_G|$) or linear mode at not to high $|V_D| < |V_G|$ the gate current I_G was dominated by electron emission both for the n- and the p-MOSFETs. In the first case I_G peaks near $V_G \approx V_D$, in the latter an I_G maximum appears at low $|V_G| \ll |V_D|$. Similar results have recently also been found by /4/.

In both cases a degradation corresponding to negative charges near drain appeared with a V_G-dependency which did not follow the I_G - V_G curve. The maximum of the degradation roughly coincided with the maximum of the substrate current. There the field in the pinch-off region near drain produces the strongest carrier multiplication.

For the first time both in n- and in p-MOSFETs also hole emission could be observed by the direction of I_G and hole trapping, albeit under extreme stress conditions? at very high V_D in n-MOSFETs for $V_G < 0$ and in p-MOSFETs for $|V_G| > |V_D|$, respectively.

The observed effects are explained by considering the 2-dimensional (oxide) field distributions and the corresponding flow of the emitted carriers near drain, the different emission probabilities and the nonuniform trapping of electrons and holes in the oxide, as well as the generation of interface states.

/1/ P.E. Cottrell, R.R. Troutman, T.H. Ning, IEEE ED-26, 4, 520 (1979)
/2/ R.B. Fair and R.C. Sun, IEEE ED-28, 1, 83 (1981)
/3/ K.K. Ng, G.W. Taylor and A.K. Sinha, IEEE ED-29,8, 1323 (1982)
/4/ K.K. Ng and G.W. Taylor, Device Research Conference, Colorado State University, Ft. Collins, Co., June 1982

Processing dependence and structure of hole traps in SiO_2

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It is known that high temperature annealing of oxidized Si samples in dry N_2 reduces the density of electron traps related to the presence of water, but introduces at the same time shallow electron traps and hole traps (1,2,3). We have reported that annealing in O_2 removes shallow electron traps and also the deep electron traps of low cross section (10^{-19} cm^2) which remain after the N_2 anneal, without reintroducing the water related traps. These results suggest oxygen deficiency as the cause of the centers (4).

In the present investigation the hole trapping behavior of such films was studied. Using the avalanche injection method it was shown that the densities of shallow and deep electron traps measured after N_2 annealing and the densities of the hole traps are comparable. Moreover, they vary in the same manner during high temperature N_2 and O_2 annealing steps. This behavior suggests that the same center, most likely trivalent silicon, is responsible for hole trapping and electron trapping in N_2 annealed samples. As expected, a reduction in the density of the traps by O_2 anneal leads to increased radiation hardness.

1. A. Hartstein and D.R. Young, Appl. Phys. Lett., 38, 631 (1981)
2. D.R. Young, E.A. Irene, D.J. DiMaria, R.F. DeKeersmaecker and H.Z. Massoud, J. Appl. Phys., 50, 6366 (1979)
3. J.M. Aitken and D.R. Young, IEEE Trans. Nucl. Sci., NS-24, 2128 (1977)
4. M. Aslam, M. Maier, P. Balk and D.R. Young, paper presented at ESSDERC (1982), Munich.

Oxide Charging and Interface State Generation by Tunnel Injection and Co-60-Irradiation Experiments on MOS Structures

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New results of high field tunnel injection and irradiation experiments on MOS structures are presented. They have been obtained from samples of different preparation conditions (wet and dry oxidation, oxidation and annealing at various process temperatures, various oxide thicknesses).

Measurements of the build-up of oxide charge and interface state density yield further confirmation of a model recently established by the authors /1/. The model of charge build-up during tunnel injection takes into account the electron-hole pair generation by inverse Auger scattering of hot electrons, the hole trapping in neutral oxide states, the subsequent electron trapping in now positively charged states and detrapping of captured electrons by electron impact ionization. By fitting the model parameters to the experimental results, the trapping and detrapping cross-sections and their field dependencies are obtained.

The generation of interface state densities is quite similar for both experiments. The generated D_{it}-distributions show a peak value at $(E - E_i) = 0.15$ eV.

There is strong evidence that the interface state density is proportional to the number of trapped holes and not to the net fixed oxide charges.

For high injection levels, a single characteristic cross-over point of all the high frequency C(V)-curves occurs. The character of the interface states can be deduced, namely acceptor type states above and donor type states below midgap. These results can also be shown for the case of ionizing irradiation by a sequence of irradiation and injection experiments.

/1/ M. Knoll, D. Bräunig, W.R. Fahrner
IEEE Trans. NS-29, Dec. 1982

DISCHARGE OF TRAPPED HOLES IN SILICON DIOXIDE

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It is known that holes introduced into the SiO_2 layer of a MOS structure are deeply trapped near the Si-SiO_2 interface[1]. The trapping sites being close to the interface is possible to observe their discharge by hole tunneling into the silicon. In the present work the discharge characteristics of trapped holes are experimentally and theoretically investigated in order to obtain the energy and spatial location of the traps.

Measurements are performed on MOS capacitors (poly-Si gate; 100 to 250 Å thick SiO_2 ; n-type Si). Hole avalanche injection from the Si substrate is used to introduce holes into the oxide. As the injection is stopped a constant bias voltage is applied to the sample and the flat-band voltage shift ΔV_{fb} is recorded (measurement time less then 50 msec) at fixed time intervals. ΔV_{fb} is found to decrease logarithmically with time in a large range of electric field and temperature (fig.1 and 2). The slope of the normalized ΔV_{fb} - logt plot is an increasing function of both electric field and temperature. The experimental results are explained in term of a modified thermal assisted tunneling model derived from the discharge theory of MNOS structures[2], including the effects of electric field and non-uniform spatial distribution of positive charge within the oxide. The analyses shows that holes are trapped in a small region (25 to 50 Å from the Si-SiO_2 interface) at an energy of about 3eV from the oxide valence band.

Similar experiments are in progress to investigate the behavior of positive trapped charge generated by high-field stressing.

1) D.J.Di Maria, D.A.Weinberg, and J.M.Aitken, J.Appl.Phys. 48, 898 (1977)

2) K.Yamabe and Y.Miura, J.Appl.Phys. 51, 6256 (1980)

INTERFACE COMPOSITION OF THIN SILICON NITRIDE AND OXYNITRIDE FILMS AS PREPARED BY DIFFERENT GROWTH TECHNIQUES

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With the continuing reduction of layer thicknesses in device structures, interfaces have an increasing influence on the ultimate behaviour of IC's. In general, the way the films are formed will determine the chemical composition of the interfaces and therewith the electronic properties of the resulting structures. This presentation focuses on the chemistry of interfaces.

Silicon nitride is chosen as an example to demonstrate how large the differences in interface composition may be when different growth techniques are applied. We will compare nitride layers formed by low-pressure chemical vapour deposition at 820°C, by plasma-enhanced chemical vapour deposition at 360°C, by thermal nitridation of silicon around 1000°C and by low-energy N_2^+ ion implantation in silicon at room temperature.

In view of the rapidly growing interest in thermally nitrided silicon dioxide we will also report on the peculiar structure that is formed upon annealing of SiO_2 in ammonia and on the kinetics of this nitridation process.

Since we are dealing with thin layers (10-1000Å), the desired compositional information can best be obtained by applying thin film analysis techniques. In particular we have used Rutherford backscattering spectrometry and Auger electron spectroscopy, the latter technique in combination with ion sputtering. With both techniques in-depth profiles of layer structures can be obtained with a good depth resolution. From the Auger spectra mainly qualitative information is derived, whereas RBS provides more quantitative data. This makes these two techniques fairly complementary and hence the combination a powerful tool for compositional characterization of layer structures as occurring in integrated circuits.

Analysis of Silicon oxynitride films using AES, RBS, the resonant nuclear reaction $^{1}H(^{15}N, \alpha\gamma)^{12}C$ and ellipsometry.

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Silicon oxynitride (SiO_xN_y) films have been grown on silicon by an LPCVD process from mixtures of SiH_2Cl_2, N_2O and NH_3 at 820°C. The oxygen/nitrogen concentration (O/N) in the film can be varied by adjusting the N_2O/NH_3 gas flow ratio. Apart from two thin (1-2 nm) oxygen-rich regions at the surface and at the Si/SiO_xN_y interface, originating from oxidation in the ambient, O/N is constant throughout the film, as deduced from AES depth-profiling measurements. Both the thickness and O/N in the film can be derived reliably from ellipsometrical measurements at λ = 632.8 nm. The chlorine concentration in the films was measured using RBS and found to be 0.15 at % for pure Si_3N_4 and 0.4 at % for O/N = 1. The hydrogen concentration in the bulk of Si_3N_4 films amounts to 3-4 at % as follows from hydrogen depth-profiling measurements by means of the resonant nuclear reaction $^{1}H(^{15}N, \alpha\gamma)^{12}C$. However, hydrogen depleted regions of 10-40 nm wide were detected at the surface of pure Si_3N_4 films as deposited. Annealing in vacuo after deposition results in a lower hydrogen contents. These depletion effects are smaller for films which contain oxygen. The hydrogen concentration in the as deposited films is smaller for O/N > 0.4. The flat-band voltage shift upon electrical stress at 300°C is lower with larger oxygen contents in the films.

Thickness Determination of Thin Oxides in MOS Structures

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When the size of Si-MOSFETs is scaled down the thickness of the gate oxide must also be reduced. The goal of this paper is to elucidate the problems appearing with the determination of the oxide thickness being smaller than 10 nm. Five different methods have been used to obtain information about the dimension of the dielectric layer between the bulk Si and the poly-Si as the gate electrode: C-V measurement, measurement of the Shubnikov-de Haas oscillations (SdH) at 4,2 K, Fowler-Nordheim tunneling (FNT), ellipsometric method and transmission electron microscopy (TEM) of thin cross sections. It will be shown that the results for the layer thickness include especially in the C-V and SdH methods the average distance of the electrons from the silicon surface, d_{el}. Thus these two methods yield the so called effective oxide thickness, whereas from ellipsometry and from TEM using lattice fringe imaging the width of the oxide without d_{el} is obtained. Furthermore it will be shown that beyond the last two methods also the FNT can be successfully used for the determination of the oxide thickness. To get the most probable value of the thickness for the SiO_2 layer, for the transition region SiO_x and for d_{el} all five methods have been applied on the same sample. It will be shown that the quantum mechanically determined d_{el}, which is of the order of 2 nm in Si, is in good agreement with the data obtained by these analyses and that the transition region SiO_x between Si and SiO_2 extends only two or at most three atomic layers.

LOW TEMPERATURE FABRICATION OF GOOD QUALITY MIS STRUCTURES ON SILICON USING ION BEAM TECHNIQUES INCLUDING H-PLASMA TREATMENT

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Ion beam techniques, combining insulator deposition and hydrogen plasma treatment, have been used for the fabrication of Metal-Insulator-Silicon structures. Relatively low interface state densities are obtained for various insulating layer materials and with a processing temperature that never exceed 300°C.

SiN_xO_y and AlN_xO_y alloys are deposited onto the silicon substrate by sputtering either a silicon or an aluminium target with a nitrogen-oxygen ion beam. Introduction of pure oxygen in the vicinity of the substrate is also used to control the y/x ratio if necessary. Starting with a good base vacuum (less than 5×10^{-8} Torr), the film composition can be controlled between pure oxide and nearly pure nitride (y less than .2).

In situ hydrogen plasma treatment of the silicon substrate prior to the insulator deposition is performed by supplying the deposition ion gun with pure H_2 gas. The H-atom beam is directed at the target from which it is merely reflected toward the substrate.

The insulating properties of the films are improved upon increasing the y/x ratio. For pure oxides, the resistivity and the dielectric strength of the insulator typically exceed 10^{+16} Ω.cm and $2\times10^{+6}$ V.cm^{-1} respectively.

For samples with no H-plasma treatment a very large density of interface states is found (N_{ss} = 2 to $4\times10^{+13}$ cm^{-2} ev^{-1} around midgap). After annealing at 300°C in nitrogen, N_{ss} is reduced in the range 5 to $10\times10^{+12}$ cm^{-2} eV^{-1}.

For H-plasma treated samples nearly perfect C(V) curves are obtained after annealing in nitrogen at 300°C during 30 mn. Frequency dispersion as well as hysteresis are barely observable. The midgap density of states is below 10^{+11} cm^{-2} eV^{-1} and flat band voltage is about 2 V, which corresponds to a total interface charge in the range 2 to $4\times10^{+11}$ cm^{-2} in flat band conditions. The changes observed in the interface state distribution consecutive to H-plasma treatment and low temperature annealing in nitrogen, are interpreted on the basis of the formation, weakening and strengthening of Si-H bonds.

Spectroscopic Studies of Electronic Conduction in SiO_2 and Si-rich SiO_2

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We have studied light emission as a probe of electronic conduction processes in both stochiometric SiO_2 and silicon rich (Si-rich) SiO_2. Experiments were conducted on electron injector structures in which a layer of Si-rich SiO_2 facilitates the injection of electrons into the SiO_2 conduction band at high current densities and relatively low average electric fields. Electroluminescence in these devices was observed to arise both from the bulk of the oxide, as reported by others[1], and from the metal counter electrodes.[2]

Luminescence from the electrodes is excited by electrons entering the metal from the SiO_2 with energies well above the metal Fermi level. The electrons loose some ot their energy to surface plasmon polaritons. These surface modes become radiative if the electrode is suitably roughened or textured. We purposely introduce roughness on some device substrates, thus allowing the plasmon mediated component of the emission to be distinguished from any other source of luminescence. The emission spectrum is then very sensitive to the energy distribution of the electrons entering the electrode. For aluminum electrodes, surface plasmon polaritons are well defined excitations at all energies up to at least 10 eV, and are thus a useful probe of electronic processes over this wide range. A linear high energy cutoff in the luminescence spectrum marks the average energy with which electrons enter the metal.

Using this spectroscopic technique we have obtained the first direct evidence for strong electric field heating of conduction band electrons in SiO_2. We find that electrons are heated to average energies of ~1 eV above the bottom of the conduction band at oxide fields

of 4 MV/cm. This increases to ~2.5 eV at 9 MV/cm. Although these results contradict theoretical models which predict little heating above the longitudinal optical phonon energy of 0.15 eV, they are in astoninshingly good agreement with inferences from many dc transport experiments.

In another application we have confirmed a model for conduction in Si-rich SiO_2 based on direct tunneling between the silicon inclusions or islands in this material. In this case electrons enter the electrode with much lower average energies than is the case for stochiometric SiO_2.

It is clear from our results that studies of surface plasmon polariton mediated luminescence are a valuable adjunct to older methods of studying electronic transport in wide band gap insulators. Future improvements in both sample preparation and detection apparatus should make it possible to study velocity run-away, impact ionization, and other phenomena of great interest.

1. P. Solomon and N. Klein, *J. Appl. Phys.* 47, 1023 (1976). C. Falcony, Doctoral Dissertation, Lehigh University (1980), *unpublished*.

2. T.N. Theis, J.R. Kirtley, D.J. DiMaria and D.W. Dong, *submitted to Phys. Rev. Lett.*.

ELECTROLUMINESCENT MIS STRUCTURES INCORPORATING LANGMUIR-BLODGETT INSULATING FILMS

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ABSTRACT

The introduction of minority carriers into the luminescent region of a semiconductor is a necessary prerequisite for radiative recombination in most electroluminescent (EL) devices. In the majority of cases this is achieved using a p-n homojunction where the minority carrier injection ratio (γ) is inherently very high. However, an alternative method must be sought for semiconductors which do not exhibit both p- and n-type conductivity (e.g. many group II-VI compounds). One possibility is to use a metal-semiconductor (Schottky barrier) structure. In such a device γ is known to be small, but it has been shown[1] that this can be substantially increased by the incorporation of a thin insulator between the semiconductor and the metal electrode. The Langmuir trough technique[2] provides an excellent method for depositing thin, uniform insulating films of controllable thickness, and can therefore be used effectively in the investigation of metal-insulator-semiconductor (MIS) EL devices. In this paper we describe the electrical and optical properties of MIS diodes incorporating various insulators deposited using the Langmuir trough technique. We show that the insertion of the organic film produces a change in the barrier height and also a substantial increase in the electroluminescence efficiency. For GaP diodes the optimum occurs at a thickness well above that predicted on the basis of simple quantum mechanical tunnelling. Similar results are also presented for structures based on large area films of ZnS. For both semiconductors a range of novel Langmuir-Blodgett materials have been used.

1. H. C.Card and E. H. Rhoderick, Solid State Elec., 16 (1973), 365.

2. G. G. Roberts, Proc. Erlangen Conference on Insulating Films on Semiconductors (Springer-Verlag, 1981, ed. Schulz) p. 56.

ELECTRIC FIELD AND TEMPERATURE DEPENDENCE OF $\mu\tau$ FOR PHOTO-INJECTED ELECTRONS IN SiO_2

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In an earlier attempt to determine $\mu\tau$ from voltage dependence of photocurrents in MOS structures $\mu\tau$ was assumed to remain constant over the whole field range studied (10^4 - 5.10^5 V/cm) [1]. Later works of R.C. Hughes [2][3] proved however, that at fields $E > 2.10^5$ V/cm $v_d = \mu E$ is no more linear in SiO_2 and μ decreases with increasing applied field.

Temperature dependence of photocurrent-voltage characteristics and photoemission yield has been studied on Si-SiO_2-Al MOS structures with 0,1 - 2,5 µm thermally grown SiO_2. An original method to evaluate $\mu\tau$ directly by comparing photocurrents measured on MOS structures with different oxide thicknesses but at the same field E and under identical optical excitation conditions was proposed and employed to determine temperature (between 77 and 300 K) and electric field dependence (between 10^4 and 5.10^6 V/cm) of $\mu\tau$.

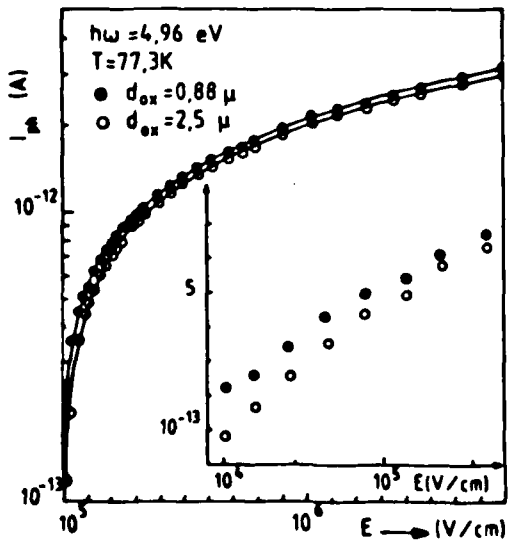
To perform a correct normalization of the injected photocurrents a modification of the "barrier-controlled photoinjection model" [4] is proposed :

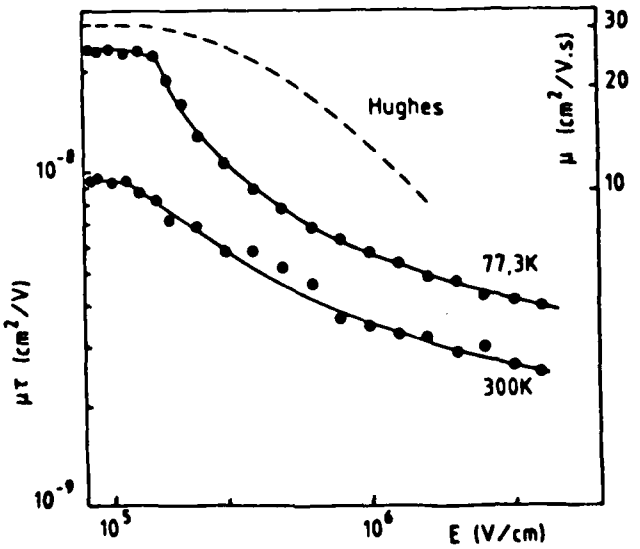
$$I_{ph} = A(\hbar\omega)\left(\hbar\omega - E_{b_0}(T) + DE^{1/2}\right)^P . \exp\left(-\left(\frac{E_0}{E}\right)^{1/2}\right) . \exp\left(-\frac{d}{\mu\tau(E,T).E}\right)$$

where $D = \left(\frac{q}{4\pi k\varepsilon_0}\right)^{1/2}$, $E_0 = \frac{q}{16\pi k\varepsilon_0 l^2}$, I_{ph} is the measured photocurrent, $A(\hbar\omega)$ is a factor depending on optical properties, $Eb_0(T)$ "zero-field threshold" depends of temperature at low impurity concentration ; ($n \simeq 10^{15}cm^{-3}$).

As carrier life time τ is considered independent of temperature between 100 and 300 K and of field up to $E = 5.10^5$ V/cm [2][3] we found interesting to compare our $\mu\tau(T)$ and $\mu\tau(E)$ experimental results to $\mu(T)$ and $\mu(E)$ experimental values of [2][3] and to $\mu(T)$ dependence deduced from the Thornbeer-Feynmann theory of electron scattering from LO phonons [5].

References : [1] A.M. Goodman, Phys. Rev. 144 (1966) 588
[2][3] R.C. Hughes Phys. Rev. Lett. 30 (1973) 1333 and 35 (1975) 449
[4] C.N. Berglund, R.J. Powell, J. Appl. Phys. 42 (1971) 573
[5] Thornbeer, R.P. Feynmann, Phys. Rev. B1 (1970) 4099





ELECTRICAL PROPERTIES OF DOPED SEMI-INSULATING POLYCRYSTALLINE SILICON

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Semi-insulating polycrystalline silicon (SIPOS) films have been shown to consist of small quasi-intrinsic silicon crystals embedded in a silicon dioxide matrix. Electron transport proceeds by tunneling of thermally generated electrons through the oxide layers separating adjacent grains. The electrical conductivity thus varies approximately exponentially with the oxygen content, while its temperature dependence resembles that of intrinsic silicon. In the present work we report on the effects of ion implantation on the temperature dependence of SIPOS conductivity. Implantation of phosphorus or arsenic in excess of the concentration required to fill the surface states at crystalline boundaries decreases the temperature dependence of the conductivity, while its dependence on oxygen content remains essentially the same as in unimplanted samples. Boron implantation does not affect the conductivity, presumably because of segregation of the dopant to the grain boundaries. When a critical implantation dose is exceeded the silicon grains become amorphised and remain so even after thermal annealing. Under these conditions the temperature dependence of the conductivity approaches that of amorphous silicon.

LIQUID-INSULATOR-SEMICONDUCTOR SYSTEMS

Dr.Ir. P. Bergveld and Dr.Ir. L. Bousse

With the development of Chemically Sensitive Electronic Devices (CSED's), a new class of semiconductor devices has come into existance, which are produced with the aid of IC technology, used as electronic components, and applied as sensors for chemical quantities.

The basic concept of these devices is the field effect principle as known from MOS devices such as the MOS transistor and the gate controlled diode. The corresponding ion sensitive devices are the Ion Sensitive Field Effect Transistor (ISFET) and the Ion Sensitive GCD. We will consider pH-sensitive devices with inorganic insulator gates, to the exclusion of devices coated with specific membranes designed to obtain sensitivity of other ions.

The early work in this field was oriented mainly to the empirical aspects such as fabrication technology, testing and development of adequate electronics. The theoretical understanding of the operational mechanisms has not progressed at the same pace. Initially the analogy with conventional well-known ion sensors, such as the glass membrane electrode, led to the expectation that the behaviour of the CSED's, based on the FET concept, could be explained in a similar way. The experimental data, collected mainly by groups in Japan, USA and the Netherlands could however not be explained with such a theory, based on diffusion controlled equilibria. The last years various types of models have been proposed to explain this discrepancy. Our group paid special attention to a model which is based on the reactivity of inorganic insulators in contact with electrolyte and focused on the pH sensitivity. Here it is considered that surface sites on the insulator react selectively with ions in the solution. This creates charged layers and a corresponding potential distribution in the electrical double layer in the electrolyte at the liquid-insulator interface. Kelly first explicitly suggested that this could be the main mechanism of operation of the ion sensitive FET devices, but without giving a quantitative theory. Siu and Cobbold applied the site-dissociation theory as proposed by Yates et al. in the field of colloid chemistry. Several other investigators have followed the same approach. This type of theory is also the basis of our model, which we have rewritten in terms of interfacial potentials instead of number of charges, as usual for colloid chemists. The reason of this theoretical transposition is the unique measurement ability created by the presence of the semiconductor part of liquid-insulator-semiconductor systems. All experimental data of ISFET's and similar operating devices can be reduced to the modulation of the flat band voltage of the system. This flatband voltage can very easily be measured in a cell consisting of Si-SiO_2-insulator-electrolyte, the latter containing a reference electrode. This cell is placed in a C-V measuring equipment, of a quasi static or differential type. The same set-up can be used to measure the impedance of the system, providing us with supporting data. It appears that conditions can be fulfilled such that the flat band voltage can be written as:

$$V_{FB} = \text{const.} - \psi_o$$

where ψ_o in the interfacial potential at the liquid-insulator interface, which can be expressed as follows in the case where β is high:

$$\psi_o = 2.3 \frac{kT}{q} \left(\frac{\beta}{\beta+1}\right) (pH_{pzc} - pH).$$

Here pH is the pH value of the liquid, pH_{pzc} is the pH where the insulator interface is uncharged (pzc = point of zero charge) and β is a sensitivity parameter, depending on the total number of insulator surface sites, the reaction equilibrium constants for acidic and basic surface reactions and the double layer capacitance including the Stern layer capacitance. The parameters determining β as well as pH_{pzc} are known from colloid chemistry for various insulators and using them to calculate V_{FB}, it appears that the measured values of V_{FB} as function of pH agree very well with the theory.

Another way to check the theoretical model with experimental data is the comparison of the measured small-signal impedance of a liquid-insulator-semiconductor system and the model of the impedance of the liquid-insulator interface based on the site-dissociation model mentioned above. The impedance model consists of two parallel contributions: the double layer capacitance (Gouy-Chapman-Stern), shunted by a branch containing the capacitance related to the acidic and basic surface reactions in series with the Warburg impedance.

It appears that theoretical and experimental data fit very well. The surface reactions cause the total interfacial impedance to be very low for insulators with a high surface reactivity and much larger for unreactive insulators.

A further support of the validity of the site-dissociation model applied to FET based CSED's is found in the measurement of the response time which is in the order of milliseconds. All other models being postulated in the literature can not explain this very fast response.

An open question at this moment is whether the proposed model can also explain the observed time drift of CSED's or whether these effects are artefacts of another nature, such as migration of charged species inside the bulk of the insulator. This question is still under investigation.

The energy distribution of Si/SiO_2 interface states measured in small-size MOSFET's using the charge pumping technique.

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The different techniques used for the determination of the $Si-SiO_2$ interface properties developed for MOS capacitors fail on small size transistors. The latter devices are however best suited for the evaluation of a fabrication process and allow a wider variety of stressing conditions to study $Si-SiO_2$ interface degradation.

Therefore there is an urgent need for a reliable technique which allows the determination of the energy distribution of the interface states in small size transistors.

It will be shown in this paper that the CHARGE PUMPING (CP) technique is very well suited for this purpose.

Starting from the experimentally confirmed model for the CP mechanism [1] it will be demonstrated that the different procedures which have been proposed in the past for determining the energy distribution of the interface states with this technique are incorrect, mainly because of a misinterpretation of the CP mechanism.

However, in this paper a variation of the CP technique will be presented which allows the correct determination of this energy distribution by directly controlling the electron and hole emission from the states during a CP cycle. The results of this adapted technique are in good agreement with those obtained with conventional techniques on capacitors, whenever such a comparison is possible.

In addition to its previously demonstrated capabilities [1,2] this new feature makes charge pumping into a powerful, fast and reliable technique easily accessible for every laboratory.

[1] N. Beltran, G. Groeseneken, R. De Keersmaecker, H.E. Maes : paper presented at the 7th SSSDT Munich, September 1982.

[2] H.E. Maes and G. Groeseneken : paper C.2.3. presented at the 11th ESSDERC, Toulouse, September 1981.

A DLTS STUDY OF NA^+-INDUCED SURFACE STATES AT THE SI/SIO_2 INTERFACE.

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The presence of Na^+ ions at the Si/SiO_2 interface is widely known to cause gross distortions in the capacitance-voltage characteristics of MOS devices. However, it is still a highly debated question to determine whether these ions introduce surface states in the Si band gap at the Si/SiO_2 interface. Recently, it has been proposed that there are no Na^+-induced interface states (1) : traps observed by some authors (2) would rather be caused by the drifting process itself.

We have performed a systematic DLTS study of Na^+ contaminated n-type MOS structures. Oxides grown under different technological conditions were immersed into a Na^+ containing solution before metallization. Ion drifting was performed under stress electric field and temperature range varying from .1 to 1 $MV.cm^{-1}$ and 100°C up to 250°C respectively. The ion concentration at the interface $[Na^+]$ was thus varied from 10^{10} cm^{-2} up to 8.10^{12} cm^{-2}. Interface state density (N_{ss}) was determined through DLTS measurements. Indeed, contrary to other electrical characterization techniques, this method is not sensitive to surface potential fluctuations -which are quite important in our experiments- and give reliable results near the Si band edges.

The following results will be presented :

i) <u>Sodium ions do induce band tails in the Si forbidden gap</u>, i.e., introduce surface states mostly near the Si conduction band. The curve $N_{ss} = f([Na^+])$, e.g. measured at a fixed energy E_c - 85 meV, presents a strong increase at $[Na^+] \approx 2.10^{12}$ cm^{-2} for all investigated samples. For $[Na^+] < 10^{12}$ cm^{-2}, the N_{ss} increase may be hidden, for some samples, in the initial interface state density background : this may explain the discrepancies observed in the litterature (1-4).

ii) <u>These band tails are stress-independent</u> : a given Na^+ concentration, obtained under different stress conditions, give rise to a same band tail.

iii) <u>In the Si midgap region</u>, a small enhancement in the interface state density is observed. The $N_{ss} = f([Na^+])$ curves differ for samples grown under different technological conditions and are found to be stress-dependent.

(1) M. W. HILLEN and D. G. HEMMES, Solid State Electr., <u>24</u>, 773 (1981).
(2) M. SCHULZ and E. KLAUSMANN, Appl. Phys., <u>18</u>, 169 (1979).
(3) D. J. SILVERSMITH, J. Electrochem. Soc., <u>119</u>, 1589 (1972).
(4) D. J. DIMARIA, J. Appl. Phys., <u>52</u>, 7251 (1981).

DETERMINATION OF LATERAL VARIATION OF INTERFACE STATES CONCENTRATION BY SCANNED LIGHT PULSE TECHNIQUE

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By using a new measurement method, Scanned Light Pulse Technique (SLPT), the lateral variations in interface states of MIS-structures can be determined. A chopped laser beam is scanned across the surface of a MIS-capacitor with a transparent metal electrode and the charge contents of optically induced current transients is measured as function of lateral position of the laser light spot on the surface of the sample. By choosing a proper voltage across the MIS-structure, it is also possible to distinguish the variations in interface states from those in insulator charges.

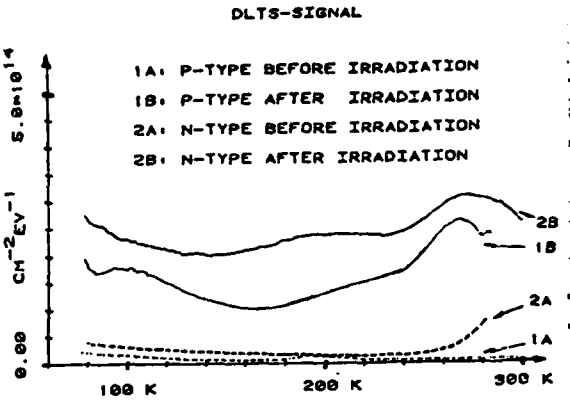

Fig. 1

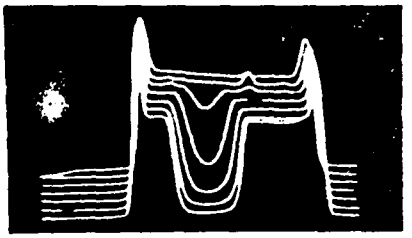

Fig. 2

Interface states were created in MOS-structures by irradiating the samples with soft X-rays. Fig. 1, which shows results from Deep Level Transient Spectroscopy before and after irradiation, demonstrates the increase of the concentration of interface states after this treatment. The SLPT-picture of a MIS-sample locally irradiated with soft X-rays is shown in fig. 2. A pronounced lowering of the SLPT-response is found in the region where a high concentration of interface states corresponding to fig 1 has been created. In fig 3, a theoretical curve for the SLPT-response, u, as a function of applied voltage, V, is compared with measured data. This measurement was made on a non-irradiated sample and the theoretical curve is fitted by our using an assumed energy distribution of interface states. The method may thus be used for local determination of such distributions.

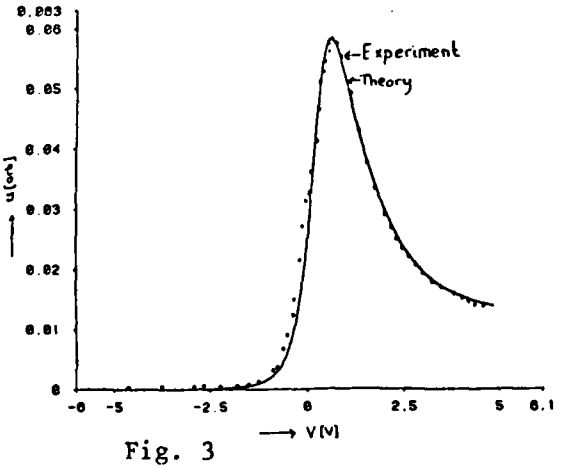

Fig. 3

The paper demonstrates the usefulness of the method for various types of insulator layers.

CONTRIBUTION OF THE Si-SUBSTRAT AND THE ANNEALING CONDITIONS TO THE Si-SiO_2 INTERFACE PROPERTIES DEDUCED FROM IN SITU WORK FUNCTION MEASUREMENTS

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Changes in work function(WF) of silicon surfaces during thermal oxidation at low oxygen pressure, have been measured by a small vibrating Kelvin probe. This method allows electrical characterization of surfaces according to their treatments, and to determine electrical state of ultra thin oxide layer ($\leq$ 40 Å) (1,2) in terms of growth conditions : oxygen pressure (10^{-1} - 10^{-3} Torr range) substrate temperature (in the 800 - 1000° C range) and material parameters (doping).

WF variations are essentially correlated to oxide thickness. The results are in good agreement with the structural model for Si-SiO_2 interface, giving five separate regions : bulk Si-disordered Si near the interface - SiO_x (one or two monolayer)-strained SiO_2 extending over 15 to 20 Å - Bulk SiO_2. In these different regions the WF variations can be explained by charge distribution or dipole contributions.

By studying the influence of the silicon doping and the growth and annealing conditions, we obtain informations on substrate, interface or oxide contribution to work function variations.

(1) J. Bonnet, J.M. Palau, E. Testemale, L. Soonckindt and L. Lassabatère
Proc. IVth Int. Conf. on Solid Surfaces, Cannes (1980)
Suppl. Le Vide, les Couches Minces 201 (1981)

(2) E. Testemale, J.M. Palau, P. Pouvil, L. Lassabatère and V.Legoascoz
Thin Solid Films 71, 161 (1980)

EXPERIMENTAL VERIFICATION OF INCREASED $D_{it}(E)$ AT THE PARALLEL EDGE OF A SURFACE CHANNEL CCD

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The small signal charge transfer inefficiency of a surface channel CCD delay line has been measured according to the method described in /1/. The independent parameter was the transfer time t, during which transfer of charge was enabled from the DC-storage gate to the clocked storage gate. The 4-phase n-channel CCD was clocked in a semi one-clock phase mode. Experiments were done on a n-channel surface CCD with double level polysilicon gates, grown on a (100) substrate with $N_A = 8 * 10^{14}$ cm-3. The channel area was laterally confined by a stopper diffusion with a surface concentration of $2.5 * 10^{16}$ cm-3. The gate length was 20 µm. For very short transfer times, $\varepsilon(t)$ is determined by the self-induced field (SIF) /2/ and given by:

$$\varepsilon(t) = \frac{T_0^2}{(t + T_0)^2} \qquad (1)$$

with T_0 inversely proportional to Q_{bg}, the background charge. For sufficiently long t, charge capture in the parallel edges becomes the dominant cause of transfer inefficiency /3/, and assuming $D_{it}(E)$ constant, it may be shown that:

$$\varepsilon(t) = -\,q\,kT\,\frac{dA(Q_{bg})}{dQ_{bg}}\,D_{it}\,\ln\frac{t}{t+T_c} \qquad (2)$$

with $A(Q_{bg})$ the channel area covered by Q_{bg}, D_{it} the trap density located at the sidewalls of the channel and T_c the clock-period. From fig. 1 it is clear that eq. (1) and (2) describe the experimental curves satisfactorily.

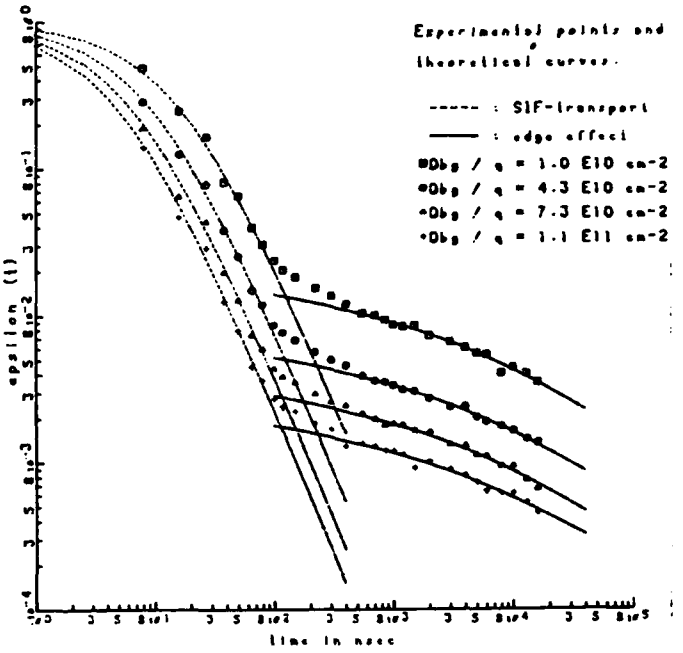

Fig. 1 $\varepsilon(t)$ for several values of Q_{bg}.

Essentially, a two dimensional calculation of two potential profile at the edge is necessary to obtain a value of $dA(Q_{bg})/dQ_{bg}$. However, by approximating the doping profile at the channel edge by a one-dimensional process simulator (SUPREM II), an estimation of $dA(Q_{bg})/dQ_{bg}$ was possible, and from eq. (2) it was found that $D_{it} \approx (1 \pm .5) * 10^{12}$ eV^{-1} cm^{-2}. This value is almost two orders of magnitude higher than the results obtained from a QSCV measurement conducted on a on-chip capacitor. These results are in agreement with /4/. At the conference more detailed data obtained from CCD's with different geometries and side-wall constructions will be shown.

References:

/1/ Wallinga, H., IEEE J. Solid State Circuits, Vol SC-14 (1979).
/2/ Lee, H.S. and Heller, L.G., IEEE Trans. Electron Devices, Vol ED-19 (1972).
/3/ Mohsen, A., McGill, T.C., Daimon, Y. and Mead, C.A., IEEE J. Solid State Circuits, Vol SC-8 (1973).
/4/ Chatterjee, P.K., Taylor, G.W., Tasch, A.F. and Fu, H.S., IEEE Trans. Electron Devices, Vol ED-26 (1979).

Direct and Fowler-Nordheim Tunneling in Thin Gate Oxide MOS Structures

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Electron tunneling through thin oxides (<150A) is being used for programming and erasing memory cells in EEPROM's. In this application, high current density (>1mA/cm2) is passed through the thin oxide by means of large oxide voltages and high electric fields (>10MV/cm). This mechanism generally makes use of Fowler-Nordheim (F-N) tunneling and has been studied extensively (1,2,3). On the other hand, it is also very important to understand the tunneling current behavior in the "direct" tunneling regime where the oxide voltage is comparable to or less than the oxide-semiconductor barrier height (~3.2eV). Direct tunneling can be encountered during the read cycles of memory cells resulting in leakage currents which can directly affect the memory cell charge retention. Also, direct tunneling will become increasingly important as MOSFET's are scaled into the sub-micron regime.

We have used the classical free-electron tunneling theory with a Franz-type two-band as well as a parabolic one-band dispersion relation in the WKB approximation to calculate the tunneling current in metal-gate MOS capacitors for injections from both Al-gate and Si-substrate. We shall show that both these dispersion relations predict the current-voltage behavior quite satisfactorily in the F-N regime for oxide thicknesses ranging from 30A - 110A. We shall also demonstrate that, in the F-N regime, the two-band dispersion relation yields an equivalent result as the parabolic one-band dispersion relation,i.e., the F-N equation. However, by comparing with experimental data, we have found that in the direct tunneling regime (an oxide voltage below 3.2V) that the two-band theory provides a more accurate description of the current-voltage behavior than the one-band theory (see Figs.1a and 1b). Also in Fig.1, a comparison of this more accurate theory is made with the conventional F-N equation to illustrate the gross inadequacy of the F-N equation if used in the direct tunneling regime.

Among the important observations are: (A) Under F-N tunneling process for oxide thicknesses ranging from 108A to 54A, the "apparent" barrier height is observed to decrease (see Fig.2). (B) Current oscillation around the F-N curve occurs for both Al-gate and substrate injections as the tunneling process approaches the "direct" regime (see Fig.3). (C) The current level changes much slower as a function of oxide field under "direct" tunneling than under "F-N" tunneling. (D) Electrons with energies of many kT/q's below the metal Fermi level will still contribute appreciably to the total current in the "direct" tunneling regime. (E) For substrate emission, tunneling by silicon valence-band electrons becomes significant at oxide voltages between 1.1V and 3V.

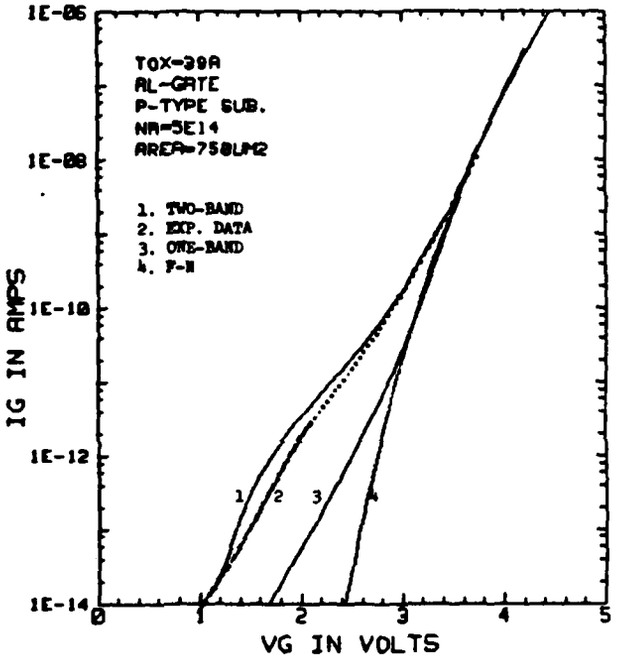
References

(1) Z. A. Weinberg, "On Tunneling in Metal-Oxide-Silicon Structures", J. Appl. Phys. 53(7), pp5052-5056, July 1982.

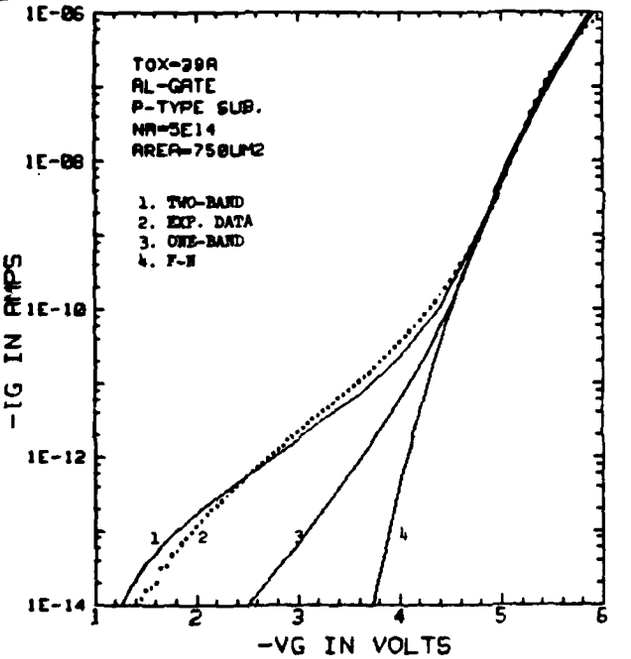
(2) M. Av-Ron, M. Shatzkes, T. H. DiStefano and R. A. Gdula, "Electron Tunneling at Al-SiO2 Interfaces", J. Appl. Phys. 52(4), pp2894-2908, April 1981.

(3) G. Krieger and R.M. Swanson, "Fowler-Nordheim Electron Tunneling in Thin Si-SiO2-Al Structures", J. Appl. Phys. 52(9), pp5710-5717, September 1981.

Fig.1 Comparison of tunneling data with theories in the "direct" tunneling regime of a MOS structure.



(a) Substrate emission



(b) Al-gate emission

Fig. 2 The "apparent" barrier height reduction (slope $\propto \phi_b^{3/2}$)

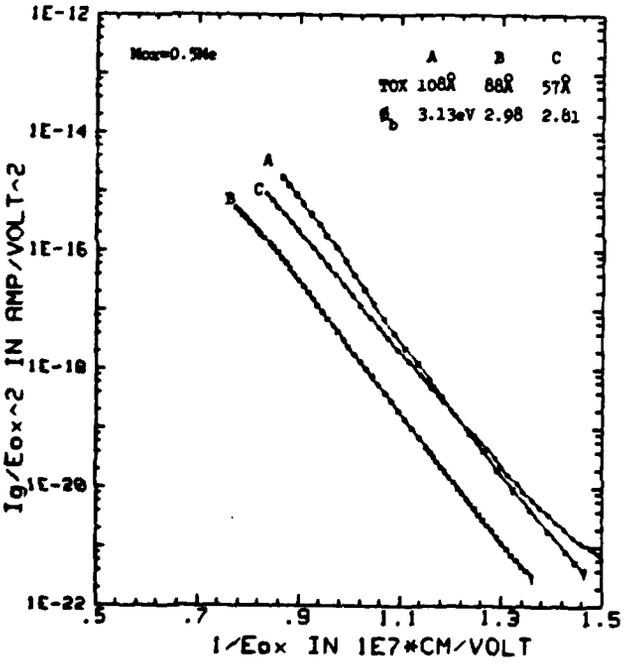
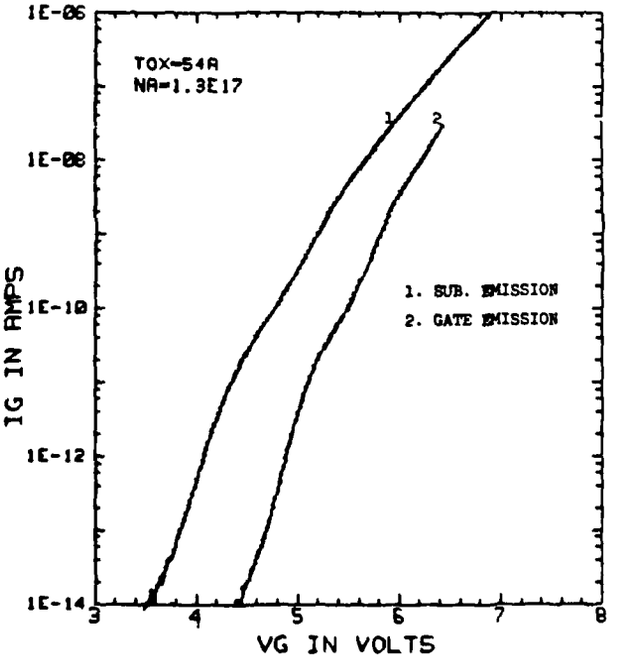


Fig. 3 Current oscillation due to electron wave interference effect.



HIGHLY UNIFORM TUNNEL SiO_2 LAYERS ON SI OBTAINED BY CHEMICAL ETCHING

Ph. GED, M. H. DEBROUX and J. P. PANABIERE.

Up to now the use of tunnel effect in devices such as electrically erasable memory or solar cells is still limited by the stability of the dielectric layer and the growth process controle.

The main difficulty in using tunnel structures is that the current flow through the insulator varies like the exponential of the thickness giving for example a ten time current increase for a 2 Å thickness variation on a 40 Å thick SiO_2 layer (1).

In this paper we present a chemical etching technique of thermally grown oxide layers. Starting from well controlled gate oxide layers of the MOS technology (500-600 Å) the oxide is gradually etched in a diluted buffered hydrofluoric acid solution at a constant temperature. Under these conditions, the SiO_2 etching rate is very uniform and typically around 7 Å/mn at 20°C. The SiO_2 thickness is monitored with the very powerful use of spectroscopic ellipsometry (2) with a sensitivity of about $\pm$ 2 Å or better in the 25-600 Å region. Furthermore, this non-destructive characterisation technique yields both thickness and structural informations on the dielectric layer.

In order to test the oxide layer homogeneity, I-V tunnel characteristics were drawn on chemically thinned layers where Al dots were evaporated. Under 1.6 V, the tunnel current on 70 % of the devices is comprised between 0.15 and 0.25 µA which corresponds to a 0.5 Å thickness dispersion on a nominally 41 $\pm$ 1 Å oxide layer over 5 cm^2, assuming the I-V curve dispersion is only due to oxide thickness variations. These homogeneity figures cannot be obtained by the direct growth of a 40 Å layer while it is interesting to note that the oxide layers of MOS technology we have used are far more uniform.

1. J. MASERJIAN, J. Vac. Sci. Technol., 11, 996 (1974).
2. Ph. GED, A. VAREILLE and D. BOIS, Thin Sol. Films, 91, 327 (1982).

ELECTRON AND HOLE CONDUCTION IN THE METAL/TUNNEL-OXIDE/N-SILICON STRUCTURE

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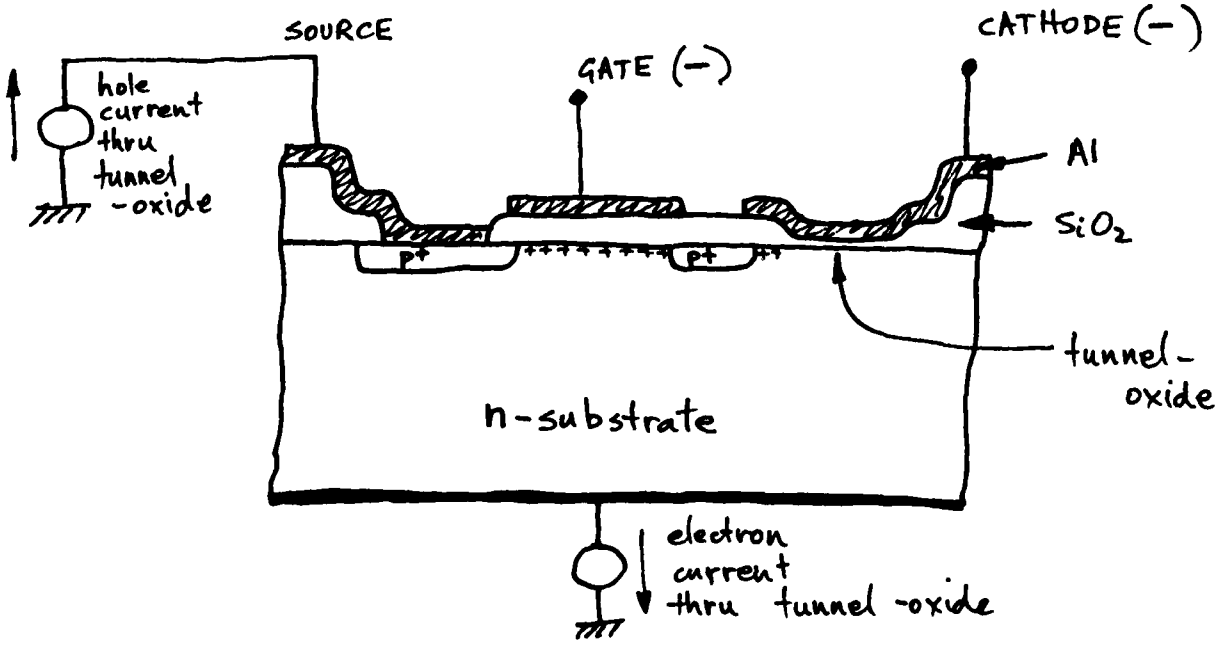
A novel device structure incorporating a p-channel MOSFET adjacent to an MOS tunnel-oxide structure is proposed as a tool for separating electron and hole current in semi-insulating films. With the P-MOSFET in saturation, the electron and hole tunnel currents can be directly measured at the substrate and source terminals, respectively (see Fig. 1). In this paper, we shall present experimental results on 15-20 Å SiO_2 films, which are typically used in MOS solar cells and Metal-Insulator-Semiconductor Switching (MISS) device [1]. Both of these device structures rely on minority carrier injection to the Si-SiO_2 interface for their operation.

The experimentally determined electron and hole tunnel current relation suggests enhanced hole conduction in the tunnel-oxide. The large-signal current gain (defined as the ratio of electron to hole tunnel current) of the oxide is always less than unity, and decreases with increasing oxide thickness and with increasing levels of minority carrier injection up to 0.3 A/cm^2. By correlating theoretical calculations with experimental results, it was found that a "thick-oxide" MOS model was still appropriate for the tunneling MOS structure. In particular, using a trapezoidal tunneling barrier and a carrier effective mass of 0.5 M_o, the electron and hole barrier heights were determined to be 3.2 eV and 3.7 eV, respectively, for 20 Å SiO_2 films. This corresponds to an oxide band-gap of 8.0 eV which is within the range used for thick SiO_2.

References:

1. J. G. Simmons and A. El-Badry, Solid-St. Electron. 20, 955 (1977).



Material and Electrical Properties of Thin (10nm) SiO2 Films Nitrided in Low Pressure Ammonia

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Thermally-nitrided silicon dioxide films have received considerable attention recently for potential application to scaled MOS-IC structures. In this paper, we present results from various characterizations of thin (10nm) nitrided-oxide films, with emphasis on their physical and chemical structure and electrical MOS properties.

Nitrided-oxide films were produced by first growing 10nm of dry SiO2 in low pressure O2 (10 Torr), then nitriding in pure, low pressure NH3 (1 Torr) at temperatures ranging from 900 C to 1050 C. The ellipsometric film thickness was not changed by any of the nitridation conditions (refractive index fixed). Film composition was determined by Auger Electron Spectroscopy (AES), Rutherford Backscattering Spectrometry (RBS), chemical-etch rate and re-oxidation resistance. These techniques indicate that nitrogen is incorporated into the oxide primarily at the outer surface and at the Si-SiO2 interface. The concentration of nitrogen at the outer surface increases monotonically as a function of both time and temperature, while the number of nitrogen atoms at the interface appears to saturate at long times and/or high temperatures. Chemical bonding in the films was examined by using AES peak shape analysis (Si-LVV) and Electron Energy Loss Spectroscopy (EELS). These analyses indicate that the films are comprised of three distinct regions: a thin oxynitride region at the outer surface, an oxide-like bulk region, and a thin nitride-like region at the interface. This hypothesis is corraborated by results obtained from a variation of the re-oxidation experiment, in which the outer surface layer (nitrogen-containing) is removed before the re-oxidation occurs. An overall model will be discussed which provides details and quantitation of the incorporation of nitrogen into SiO2.

Electrical measurements were performed on MOS capacitors and FETs which incorporated nitrided-oxide dielectrics with relatively mild nitridation treatments ($\leq$ 950 C, $\leq$ 2 hr). Typical MOS parameters were extracted from the measurements and were found to be comparable (within 20%) to those obtained from equivalent devices with non-nitrided SiO2 dielectrics. Parameters which were examined include: 1) position of flatband voltage relative to "ideal", 2) fast interface state density, 3) I-V characteristics through the films, 4) average breakdown field, 5) electron trapping characteristics and 6) low field FET mobility. The most outstanding observed difference between the oxide and the nitrided-oxide films was the ability of the latter to inhibit diffusion of boron (from a p+ poly gate electrode) throughout the entire course of a MOSFET fabrication sequence. Electrical measurements are currently being performed on nitrided-oxides with more extreme nitridation treatments and will be reported.

TUNNEL-BARRIERS AND ADMITTANCE OF SEVERAL VERY THIN INSULATORS IN Au-MIS PHOTODIODES ON p-SILICON

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The deposition of Au on p-silicon by DC-sputtering causes a considerable increase of the barrierheight ($\phi_B \approx 0.65$ eV as determined by Fowler-plots) compared with evaporated contacts ($\phi_B \approx 0.25$ eV). A majority-carrier MIS device will be formed which allows us to study interfacial states and tunneling behavior. Thin insulators will not be attacked by the non-reactive Au.

Different interfacial layers have been used: thermally grown oxides, the residual layer left on the surface after an HF-etch and after a soke in a solution of fluosilicic-acid (S.F.A.). For all structures high tunneling barriers for electrons ($\chi_e^{\frac{1}{2}}$ d = 20.....30) and low barriers for holes ($\chi_h^{\frac{1}{2}}$ d < 4) were found. An in-situ ellipsometrical study has shown that only with the S.F.A.-treatment of the surfaces a layer of 1,6 nm could be deposited in a very reproducible way. Photovoltaic test-devices in which this layer has been used show a good performance ($I_{sc} \approx 20$ mAcm^{-2}) and stability (although not optimized as solar cell), which is not the case for the thermal oxides.

The usual high density of interface-states for thin thermal oxides around midgap ($N_s \approx 4.10^{12}$ cm^{-2}eV^{-1}) is halved when the surface have been in contact with mentioned etching liquids. This can be interpreted as the result of fluorine-incorporation in these layers.

Finally besides sputtering of noble metals (Au,Pt), more reactive metals (Cu,Ag,Pb) have been used. In the latter case higher interfacial barriers were found, which is evidence of additional oxidation during the metal deposition.

CONDUCTING ANODIC OXY-FLUORIDE LAYERS ON SILICON FOR MIS-SOLAR CELLS

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MIS-solar cells on p-silicon are currently prepared by thermal oxidation to form an insulating layer of 2 nm. The preferred metal Al (low workfunction) however, attacks this layer forming Al-oxide and leaving behind Si (clusters). Thicker thermal oxide layers (> 2.5 nm) do block the photocurrent of the solar cell (electron current).

The aim of this work is to increase the thickness of the insulating layer to overcome the chemical attack by applying a different oxidation method in order to maintain the photocurrent. Also to incorporate fluorine during the process for the reduction of the number of interface states (recombination) and to develop a low-temperature process in view of the application of polycrystalline silicon.

First results on this new insulating layer are:

- preparation of the layers by anodic oxidation in a water ÷ fluosilicic acid mixture gives a homogeneous layer on p-Si;
- layers have been prepared up to 50 nm, they follow a logarithmic growth rate;
- layer thicknesses, established over the range from 5-45 nm by capacitance and ellipsometry, coincide up to 25 nm, average refractive index $n \approx 2$ at $\lambda = 546.1$ nm compared to 1.5 for SiO_2 (probably because of absorption and/or different composition;
- ESCA and AES indicate the presence of F besides that of Si and O;
- the layers thus prepared have been tested with an Hg-MIS contact and show clear saturation currents ranging over 5 decades. This is interpreted as an increase of the silicon barrier by 0.3 eV due to positive charge in the layer (increasing with thickness);
- photovoltaic test cells with sputtered Au* as the metal (non-reactive) show an almost constant photocurrent up to 20 nm layer-thickness compared with a reduction of the diode current of about 1.5 decade;
- based on these results a model for the charge transport will be suggested.

Application of the reactive Al-metal layer has been started now, because an insulating layer of 10 nm can tolerate an attack by the Al of about 2.5 nm; results of this type of cells will be presented.

* Charge transport properties of several very thin insulating layers are investigated on Au-nSi MIS cells in our group as well

Electronic conduction and trapping in MIS system with multilayer dielectrics

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This review is concerned with the conduction in MIS systems with multilayer dielectric, used as charge storage medium in non-volatile memory devices or as stable thin gate insulator of silicon field effect transistors. In addition to its pronounced dependence on the electric field the conduction is determined by the properties of the component films, one of which is normally thermally grown SiO_2, and by the energy barriers separating the silicon substrate and the gate electrode from the adjoining dielectric. Since, with exception of thermal SiO_2, all insulators show a considerable capture rate for charge carriers, trapping and detrapping phenomena and the resulting space charge distribution are one aspect which will be discussed. The second are the effects of the injecting contacts and the energy barriers between the layers. In addition to qualitative models to describe the observed behavior the methods for physical analysis of insulator systems and for determining the dominant carrier type and the charge profile will be dealt with.

TRANSIENT REVERSIBLE CURRENTS IN MAOS STRUCTURES

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MAOS structures with a polycrystalline Al_2O_3 layer of 1000 Å thickness and a 25 Å SiO_2 film grown on n-type silicon are investigated. When a step-like electric field $E \leq 1$ MV/cm is applied a current with a time behaviour $J(t) = At^{-1}$ flows to the device in a time range from 5 µs to 5000 s. When the sample is short circuited a discharge current with the same time behaviour but opposite direction can be observed (Fig. 1). The currents are proportional to the field. From measurements of the dielectric displacement at the silicon interface it is concluded that the currents arise from bulk polarization. In order to decide whether the polarization results from a distribution of relaxation times (DRT) or any other physical mechanism [1,2,3] the short circuit currents after different lengths of the loading pulses were measured (Fig. 2) . The result is that the DRT theory should be used. The currents can be derived from a first order rate equation for the polarization: $\tau\dot{P}(t) = -(P(t)-P_\infty)$ with $\tau = \tau_0 \exp(\Delta)$ where Δ is a distributed magnitude. Since in single crystals of Al_2O_3 these currents could not be detected it is highly probable that crystal defects are related to the currents. Possible physical interpretations of Δ will be discussed.

[1] Jonscher, A.K., Hill, R.M. IEE Conf. Publ. 177, 164 (1979)
[2] Dissado, L.A., Hill, R.M.,Phil.Mag.B 41, 625 (1980)
[3] Guo, T., Guo,W. IEEE Annual Report CEIDP 1982, p.29

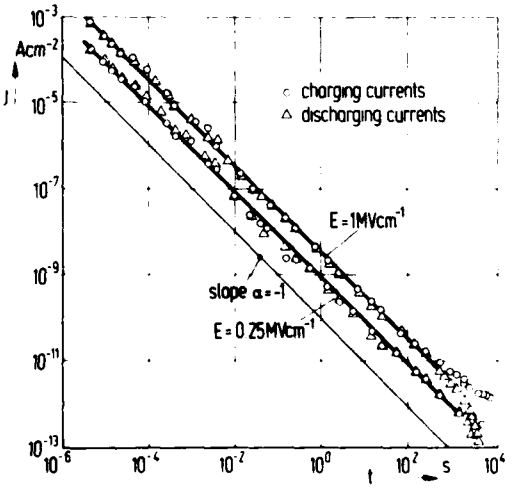

Fig. 1

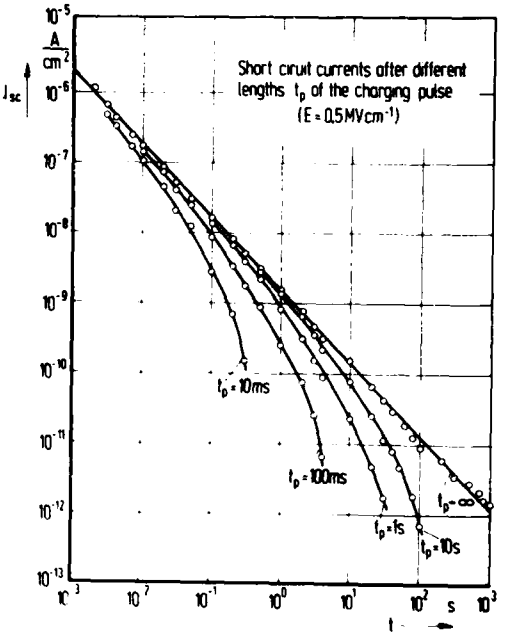

Fig. 2

Two-carrier conduction in amorphous chemically vapour deposited (CVD) silicon nitride layers.

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Silicon nitride is widely applied in the integrated circuit (IC) technology thanks to its excellent masking and passivating properties and is also used as the charge storage layer in the non-volatile metal-nitride-oxide-silicon (MNOS) memory structure.

A thorough knowledge of the physics of conduction and the trapping properties of these films is indispensable for understanding the operation and limitations of MNOS devices.

Whereas in early studies the conduction in silicon nitride was attributed to either electrons or holes depending on the polarity of the applied voltage, it was shown recently that the conduction is rather a two-carrier process.

In this paper the results of an extensive study of the conduction in nitride layers will be presented. A specially designed transistor structure was fabricated for this purpose. This structure allows the separation of electrons and holes flowing through this layer and therefore provides direct information on the relative contribution of both charge carriers to the total nitride current. This technique is used for the comparative study of the conduction of nitride layers deposited at atmospheric pressure (APCVD) and layers deposited at low pressure (LPCVD). The study was performed on NO combinations with Ultra thin oxide layers (2 nm) and with thicker oxides (8 nm), at different temperatures, for different silicon substrate types and for three different gate electrode materials, Aluminium, Gold and polysilicon. The study shows that for negative gate polarities hole conduction is dominant for both types of nitride. For positive gate polarities hole transport is dominant for APCVD nitride whereas electron conduction is also important for LPCVD nitride layers. A model for this two-carrier conduction will be presented and it will be shown that this model allows to explain the differences in behaviour of MNOS transistors fabricated with the two types of nitride layer.

Identification of charge carrier type in MIS structures with Al_2O_3 gate insulator

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Earlier studies from this laboratory showed an inverse dependence of the injection current at negative gate voltages in MAOS (Metal-Al_2O_3-SiO_2-Si) capacitors with thin SiO_2 layers on the work function of the gate metal and a preference for storing negative charge in these structures. Even though under certain conditions also positive charging occurs it was concluded that electrons dominate the conduction process in Al_2O_3 /1/. To obtain more detailed information, particularly on the possible role of holes as carriers, we carried out further studies on this problem utilizing the induced junction technique to separate electron and hole currents /2/. Both thin (2.5 nm) and thick (8.0 nm) SiO_2 films on n-and p-type Si substrates were used; the Al_2O_3 layers were pyrolytically deposited at 900°C.

In all cases only electron currents could be detected. This implies that the contribution of holes to the current was below 1%. The positive charging observed at negative gate voltage may be due to hole trapping in the insulator system near the silicon or to electron emission from the insulator into the silicon. For thick SiO_2 devices considerable generation of electron-hole pairs in the silicon by hot electrons entering this region at negative gate bias was observed. It will be shown that these findings are in agreement with a simple model based on the band structure of these MIS systems.

/1/ H. Kampshoff, F. Stephany and P. Balk, J. Electrochem. Soc. 124, 1761 (1977)

/2/ A.S. Ginovker, V.A. Gritsenko and S.P. Sinitza, Phys. Stat. Solidi, A26, 489 (1979)

INSTABILITY MECHANISMS IN AMORPHOUS SILICON - SILICON NITRIDE THIN FILM TRANSISTORS

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There has been a considerable increase of interest in amorphous silicon thin film transistors in recent years owing to their promise for application as switching elements for matrix addressing of large area displays. Many groups around the world are active in this field and transistors have been fabricated with a variety of different structures and different materials[1]. To date, the best performance is obtained with amorphous silicon - silicon nitride thin film transistors, in which first the nitride layer and then the amorphous silicon layer are deposited, by plasma - CVD, sequentially in the same growth system. Several groups have reported similar characteristics using this approach.

The main advantage of this method is that it results in a "clean" interface with a low density of interface states ($<5\times10^{11}cm^{-2}eV^{-1}$), a low density of bulk α-Si deep states near to the interface ($<10^{17}cm^{-2}eV^{-1}$) and a low density of fixed charge in the insulator near to the interface ($<10^{11}cm^{-2}$). In most cases, an additional insulating layer (nitride and oxide layers have been used) is deposited on top of the amorphous silicon for top surface passivation. Again a low fixed charge density is obtained ($<2\times10^{11}cm^{-2}$).

The transistors show a six orders of magnitude change in the source-drain current between the 'on' and 'off' states for a gate voltage swing of 15 volts (corresponding to fields in the dielectric ~ 3×10^{5} V cm^{-1}).

Apart from the basic device characteristics an important aspect of the performance of TFTs is their stability, which is a potential problem with thin film materials. In this paper we will review the present situation for amorphous silicon TFTs, and in particular, discuss the consequences and give examples of instability mechanisms which change i) the bulk density of states in the amorphous silicon and ii) the "fixed" charge density in the silicon nitride.

Reversible changes in the conductivity of amorphous silicon, produced by prolonged white light illumination and reversed by annealing to 180°C, were first reported by the RCA group[2], in connection with the stability of solar cells. Similar effects occur in amorphous silicon thin film transistors, where the conductivity changes affect the off conductance and the threshold voltage[3]. This result is due to a modification of the density of deep states in the amorphous silicon, in such a way that the bulk Fermi level is moved away from the conduction band edge (by ~ 0.1eV for a decrease in off conductance by a factor of ~ 30). Annealing to 180°C, therefore, has the exact opposite effect on the deep bulk states[3].

Prolonged bias-temperature stress causes a shift of the threshold voltage of the same sign as the gate bias, with only a small effect on the off conductance, pre-threshold conductance or the field effect mobility. This effect is due to charge trapping in the gate insulator, with charge transfer predominantly between the semiconductor and the insulator[4] [5]. The trapped charge is largely detrapped by annealing to 180°C, thus reversing the threshold voltage shift due to charge trapping as well as affecting the amorphous silicon deep states.

Thus we have an instability mechanism which is a bulk property of the amorphous silicon and another which is a property of the silicon nitride. Of the two mechanisms, the charge trapping instability is the more important for the display application[5]. However, because the fields in the dielectric are low, this threshold voltage instability is reasonably small. Typical results are: ΔV_T~1V, for a d.c. bias field of 3×10^5 V cm^{-1} applied for 6×10^4 secs at 25°C, increasing to ΔV_T ~ 7V at 100°C. The magnitude of ΔV_T is lower for negative bias.

Possible mechanisms to account for the charge transfer at low fields will be discussed.

References

(1) see for example papers in SID symposium digest 33-49 (1982).
(2) D. L. Staebler and C. R. Wronski J Appl. Phys. 51 3263 (1980).
(3) M. J. Powell, B. C. Easton and D. H. Nicholls, J. Appl. Phys. 53 5068 (1982).
(4) D. G. Ast Proc. International Display Research Conference, Cherry Hill, 152 (1982).
(5) M. J. Powell and D. H. Nicholls: IEE Proc. Part I 130 Feb. (1983).

Interface State Densities of APCVD and PECVD Silicon Nitride Films on Silicon

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Despite the importance of Si-nitride for electronic thin film devices, only a few data are available about the interface state density (N_{it}) of atmospheric pressure chemical vapor deposited (APCVD) Si-nitride films on silicon. The interface properties of plasma enhanced CVD (PECVD) Si-nitride on silicon have not been investigated up to now.
In this paper, N_{it} was studied as a function of the nitride deposition temperature and the postdeposition annealing treatement. For this purpose, Al/Si-nitride/native Si-oxide/p-Si(100) structures were prepared using both APCVD Si-nitride deposited at temperatures between 620°C and 900°C and PECVD Si-nitride deposited at temperatures between 250°C and 400°C. The interface state density was determined by the quasistatic CV technique.
For the APCVD Si-nitride samples the N_{it} values at midgap are varying with the deposition temperature T_N from $N_{it}= 4x10^{11}$ $cm^{-2}eV^{-1}$ ($T_N= 690°C$) to $N_{it}= 1.5x10^{12}$ $cm^{-2}eV^{-1}$ ($T_N= 900°C$). By annealing in nitrogen at temperatures above the deposition temperature, the interface state density is increased.
For the PECVD Si-nitride films in the as grown state the determination of N_{it} by quasistatic measurements is difficult to perform because the CV curve is shifting due to charge injection into the nitride. By nitrogen annealing of these films between 400°C and 600°C, however, the effect of charge injection is reduced. N_{it} was found to be dependent on the deposition and annealing temperature. Values for N_{it} below 10^{11} $cm^{-2}eV^{-1}$ could be reached, which are lower than those obtained for APCVD Si-nitride. Further improvement of N_{it} can be obtained by oxygen treatement of the silicon surface ($d_{ox}= 2nm$) prior to the nitride deposition.
The different dependencies of the interface state densities on the deposition and annealing temperatures obtained for PECVD and APCVD Si-nitride films will be discussed.

THE LOW-TEMPERATURE OXIDATION OF Si IN PRESENCE THE OXIDE CATALYSTS

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This study concerns the thermal oxidation of Si in dry oxygen in presence the oxide catalyst. The silicon was separated from catalyst by oxygen gap. Heavy-volatile metal oxides were used as catalysts. SiO_2 films grown with catalysts were analysed for chemical composition by the AES that revealed no doping of these films. In the presence of some oxide catalysts the thermal oxidation of Si was found to occur with acceleration. The analysis of the oxidation kinetics has shown that the acceleration is observed of both diffusion and kinetics stages.

The effects observed can be explained by the generation of excited oxygen (apparently, a singlet oxygen) from the catalyst surface. Really, at temperatures above 700 K the adsorption of O_2 molecules on semiconductor oxides is, as known, dissociative, and consequently, their desorption from these surfaces is a recombination which makes possible the generation of excited oxygen from the catalyst surface followed by the acceleration of oxidation.

HIGH FREQUENCY PLASMA ANODIZATION OF SILICON

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The growth of thick oxides at low temperature is becoming of critical interest in VLSI semiconductor devices.

Plasma anodization is a low temperature, dry process which moreover seems to be more anisotropic than thermal oxidation reducing the bird's beak effect.

Nowadays considerable work is needed for basic understanding of plasma anodization. In this work the influence of different parameters on the kinetics (thickness < 800 nm) has been studied and the oxides characterized.

The plasma is generated by external capacitive coupling of a 13,6 MHz, 1 Kw, generator to a quartz tube. The sample temperature is externally controlled. The anodizations were performed in flowing dry oxygen at $3\ 10^{-2}$ torr, at constant current (10-30 $mAcm^{-2}$), and at temperatures ranging from 500°C to 800°C. In situ thickness measurements have been obtained by reflectometry.

Depending upon plasma conditions two kinds of kinetics have been obtained. The first ones are not linear, the rate at 500°C, 30 $mAcm^{-2}$ is similar to that of thermal oxidation at 900°C in H_2O. The second ones are linear with lower rates. In each case the rate increases with temperature and current density.

The average electric field in the growing oxide increases linearly with thickness and decreases with temperature. The refraction index is similar to that of thermal oxide. Without annealing, Q_{ss} in the range of 10^{11} cm^{-2} have been deduced from high frequency C(V) curves.

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ABSTRACT

INSULATOR INTERFACES WITH $Hg_{1-x}Cd_xTe$

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The surface and insulator interfaces of (Hg,Cd)Te have been under intense scrutiny because of their importance to infrared detector operation. For such applications, it is necessary to passivate the surface of (Hg,Cd)Te in order to reduce surface leakage currents and maintain electrical and chemical stability.

However, it is difficult to effectively passivate the (Hg,Cd)Te surface. Compared with the surfaces of other semiconductors, the surface of (Hg,Cd)Te is particularly sensitive to chemical and physical treatments. The standard etching processing using bromine in methanol can deplete cations and produce a surface layer of TeO_2.[1] Irradiation with an electron beam of a few keV energy can convert the surface layer (10-100 Å) of (Hg,Cd)Te into CdTe.[2] Also, sputtering with Ar ions of 1-2 keV can change the chemical composition of the top atomic layers.[3] The crystallographic damage and deviations from stoichiometry due to these treatments increase[1] oxide growth rate; on vacuum-cleaved surfaces, the growth rate is insignificant. Thus, the activity of the surface leads to a strong (Hg,Cd)Te/passivant interaction. The nature of this interaction and its bearing on electrical parameters will be discussed for several commonly used passivants.

Because of the high-temperature instability of (Hg,Cd)Te, useful passivants are native oxides produced by excited oxygen, as in anodization, deposited insulators such as ZnS, or combinations of these. Studies of anodization of (Hg,Cd)Te in an electrolyte have been the most extensive and provide the most comprehensive picture of (Hg,Cd)Te/passivant interfaces; therefore, they will be discussed in depth.

Anodic oxides several 1000Å thick can readily be formed on (Hg,Cd)Te in an electrolyte of ethylene glycol and KOH.[5] The oxide is amorphous, consisting primarily of $CdTeO_3$ and $CdTe_2O_5$ with a small Hg content[6]. The oxidation reaction is strong enough to damage the semiconductor to a depth of ~100Å beneath the oxide interface. Examination of the interfaces by various surface spectroscopic techniques indicates that the relative concentrations of Hg and Cd (x-value) in the semiconductor play an important role in determining the properties of the interface region. For example, X-ray photoelectron spectroscopy and electrochemical polarization curves indicate that the interface region of x = 0.2 material becomes substantially depleted of Hg in the initial stages of anodization[6]; however, no such depletion of Hg is observed for x = 0.3 material. Anodic oxides contain a large fixed charge--typically 2×10^{12} cm^{-2}--which may be associated with this interface. The charge can be reduced by an order of magnitude in x = 0.3 material if the semiconductor surface is subjected to an electroetch[7] prior to anodization. These results indicate that the composition and structure of the semiconductor surface prior to oxidation have a direct effect on the resultant (Hg,Cd)Te electronic properties. Similar effects found in other passivants, such as photochemical oxides and ZnS, will also be discussed.

References

1. D.R. Rhiger and R.E. Kvaas, J. Vac. Sci. Technol. 21, 168 (1982).

2. T.S. Sun, S.P. Buchner, and N.E. Byer, J. Vac. Sci. Technol. 17, 1067 (1980).

3. H.M. Nitz, O. Ganschow, U. Kaiser, L. Wiedman, and A. Benninghoven, Surf. Sci. 104, 365 (1981).

4. P. Morgen, J.A. Silberman, I. Lindau, W.E. Spicer, and J.A. Wilson, J. Electron. Mater. 11, 597 (1982).

5. P.C. Catagnus and C.T. Baker, U.S. Patent 3,977,018 (1976).

6. G.D. Davis, T.S. Sun, S.P. Buchner, and N.E. Byer, J. Vac. Sci. Technol. 19, 472 (1981); J.S. Ahearn, G.D. Davis, and N.E. Byer, J. Vac. Sci. Technol. 20, 756 (1982).

7. B.K. Janousek and R.C. Carscallen, J. Vac. Sci. Technol. 21, 442 (1982).

ELECTRICAL PROPERTIES OF THERMALLY-GROWN SiO_2 FILMS ON N^+ POLYSILICON

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Multi-level polysilicon structures, consisting of polysilicon layers separated by an insulating dielectric, are extensively used in silicon device technology. Commonly, the LPCVD polysilicon layers are deposited at temperatures of approx. 620°C, and the inter-level dielectric consists of thermal SiO_2 grown from the underlying polysilicon. It is well known[1], that the insulating properties of SiO_2 thermally grown from underlying polysilicon are inferior to those of SiO_2 grown from crystalline, bulk silicon. In particular, poly-oxides have a lower dielectric strength and exhibit enhanced Fowler-Nordheim tunneling current for a given applied electric field. These effects have been attributed to the texture (surface roughness) of the polysilicon-SiO_2 interface[2]. In this paper, we present experimental results for both ion-implanted and diffusion-doped polysilicon films that were initially deposited in the amorphous phase or the poly-crystalline phase.

For films initially deposited in the amorphous phase, SEM photographs, UV reflectance measurements, and cross-sectional TEM photographs of the N^+ polysilicon surface after oxidation suggest a high degree of "smoothness" when compared to films deposited in the polycrystalline phase. Furthermore, the resulting electrical characteristics of the thermally-grown SiO_2 (an increase in dielectric strength and a reduction in Fowler-Nordheim tunneling current) represent a significant improvement compared to films initially deposited as polysilicon. For example, for $POCl_3$-doped films subsequently oxidized at 1000°C in dry oxygen, there was an improvement in mean oxide breakdown field from 3-3.5 MV/cm to 6.5-7 MV/cm when comparing 620°C polysilicon to amorphous silicon deposited at 560°C. Furthermore, the leakage (Fowler-Nordheim) current at any given applied field was typically 4 orders of magnitude less. Our experimental data have shown that these improvements can be achieved independent of the process used for doping the polysilicon or the process used for thermal oxidation. In addition, the electron trapping-rate in the oxide as determined from constant-current, time-dependent stressing was found to be much lower for devices with a low degree of surface roughness. The improved dielectric properties of the SiO_2 should result in an increased yield and an improvement in long-term reliability, and would allow a thinner film to be used in situations where a higher capacitance per unit area is required (for example, an on-chip integrated capacitor).

References

1. D. J. Di Maria and D. R. Kerr, Appl. Phys. Lett. 27, 505 (1975).

2. R. M. Anderson and D. R. Kerr, J. Appl. Phys. 48, 4834 (1977).

DAMAGE CAUSED BY ELECTRON INJECTION

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Continuous electron injection leads finally to the breakdown of an MOS Capacitor. In the pre-breakdown stage a dielectric is worn out by the damage caused by the injected electrons. The change in the dielectric can be observed as a generation of "traps" and "surface states". After a certain amount of injected electrons a space charge of opposite sign tends to develop. This process is called the "turn around" effect. A number of observations will be discussed exposing in some way the nature of the produced damage.
These observations are:

1) C-V curves of MOS capacitors show, apart from a shift, also an increasing hysteresis. The hysteresis is stable, it increases by injection until the dielectric breaks down (see fig. 1).

2) The frequency response of a dielectric changes after injection of electrons. The impedance then shows an anomalous frequency dependence which can not be described by a simple equivalent circuit.

3) Injection of electrons in an MOS capacitor gives rise to a photo current in an underlying pn diode. This photo current is independent of the direction of the injected current.

The observations will be shown to fit in the breakdown model of Budenstein[1] describing the growth of micro gas-discharges in dielectrics. Gas-discharges contain gaseous ionic species which may migrate over a larger distance in the dielectric and give rise to large polarisation effects as well to an increased a.c. conductance. This type of defect may cause the observed hysteresis effects and "turn around" effects as well as an apparent increase of "surface states" as will be discussed. Since micro gas-discharges may grow at various locations and stages and may differ in geometric size they will be ignited at varying frequencies giving rise to the anomalous impedance behaviour. Micro gas-discharges also emit light which fits to the observation of photo currents. Evidence supporting the existence of micro gas-discharges will be discussed and a short description of the various steps leading to dielectric breakdown will be given.

References 1) Budenstein P., Proc. IEEE, E.I., **15**, (1980) 225.

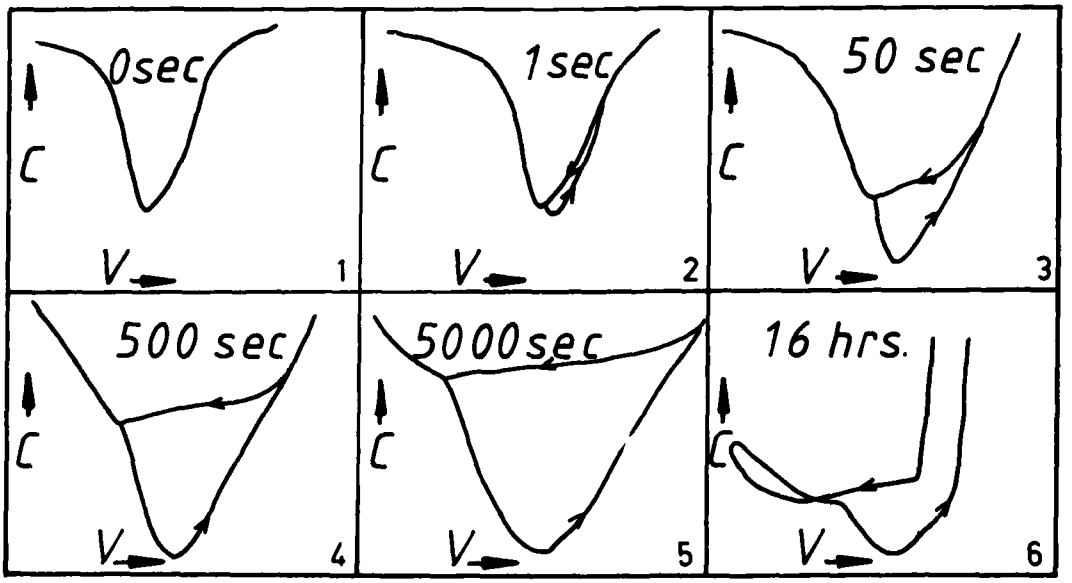

Fig. 1 C-V curves show an increasing hysteresis upon electron injection. The total stress period for avalanche injection under a

THE CHARACTERIZATION AND TECHNOLOGY OF DEPOSITED OXIDES FOR EEPROM

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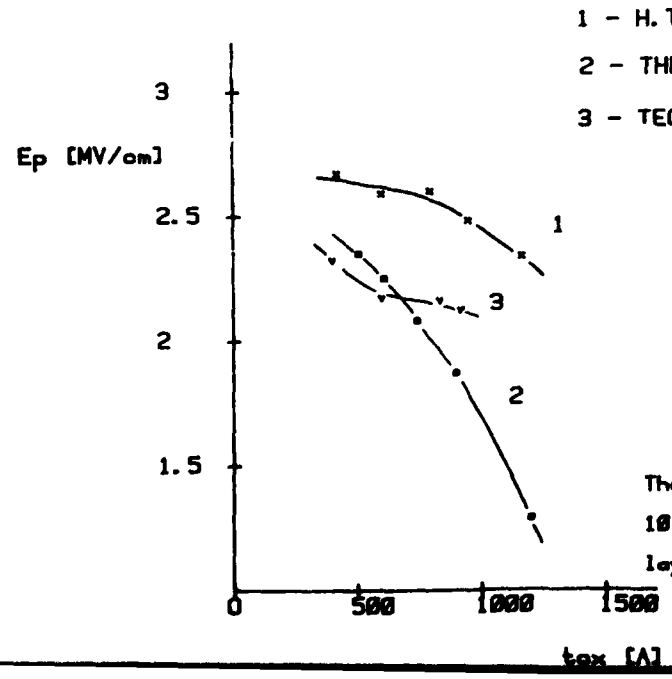
In transistors for EEPROM devices is the information stored in the form of charge on a floating gate. The requirements on the non-volatibility imply a very high resistance for the dielectrics below and over the floating gate. The oxides below the floating gate are thermally grown oxides on single crystal silicon which have intrinsically the required high resistance. However the thermally grown oxides on the poly-crystalline floating gate have a much lower resistance. Therefore deposited oxide layers were investigated and their properties compared to oxides thermally grown on poly-Si.
For the electrical characterization we used two methods, firstly the dielectric breakdown test and secondly, the oxide leakage test. In both methods the voltage is ramped and its value recorded when the current through the oxide in a MOS capacitor on poly-Si exceeds a preset value. In the first method of dielectric breakdown this current is typically 10^{-6} A/mm^2 and is accompanied by a destructive breakdown. In the second method the oxide current level is much lower, 10^{-11}/mm^2 and is non-destructive. The oxide field E_p is then much lower than the intrinsic breakdown field and it depends on the voltage polarity. The figure yields values of E_p of several dielectrics between two poly-Si layers with the top poly-Si positive (bottom poly electron injecting).
The deposited oxides were (among others) obtained by chemical vapour deposition from dichlorosilane at 920°C (HTO) or from tetraethyl ortho silicate (TEOS) at 625°C. It appeared that the value of E_p is highest for the higher deposition temperature. Also E_p increases with decreasing thickness of the thermal oxide. This can qualitatively be explained in terms of decreasing asperity size on the poly-Si.



The fieldstrength at injection current of 10 pA vs. the thickness of the isolation layer.

SOLID STATE PHYSICS USING SILICON INVERSION LAYERS

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A B S T R A C T

The inversion layer of the Si MOSFET continues to be one of the most useful model systems for the investigation of many electron transport phenomena. This use stems from the two main advantages of the system, the two dimensionality of the electron gas in the surface potential well and the control over the Fermi energy, and carrier concentration, provided by the gate voltage. In this talk a review will be presented on the optical and electrical effects which the MOS inversion layer is used to investigate. We will concentrate on those phenomena which are dependent on the quality of the interface between Si and the Silicon Dioxide, or other dielectric. The role of interfacial charges in determining the inversion layer mobility will be discussed and it will be shown that both scattering from surface roughness and surface charge are important. The nature of the interface defines the mean free path between elastic scattering collisions and this determines the temperatures at which the logarithmic corrections are observed. This effect tends to be found at very low temperatures and arises from two mechanisms, the first is the localisation of all states in two dimensions and the second is the relation between the electron-electron interaction and elastic scattering. Both these effects will be discussed and the results of experiments on the InP inversion layer will be contrasted with those obtained using Si. The nature of the electron localisation will be contrasted with that in an intense magnetic field when the Hall resistance takes quantised values.

Finally, we will present results on an effect found in the Helium range of temperatures either in the contact regions of MOS devices or in the channel after the device has been irradiated. It is found that the device conductance oscillates as a function of gate voltage. The existence of the oscillations reflects aspects of the electron potential interaction which are common for interface states and impurities. The present state of knowledge of this effect will be discussed.

Oxide breakdown at near-zero electric fields

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Oxide breakdown experiments are usually performed by applying a large electric field to an MOS capacitor. However, when the hot electron gas that exists in the high field region near the drain of a short channel n-MOS transistor is used as a source for energetic electrons entering the oxide it is possible to cause breakdown of the SiO_2 at near-zero electric fields. The gate current can be held at the desired level by adjusting the drain-source voltage, while keeping the gate-drain voltage V_{gd} constant.

Fig. 1 shows the variation of Q_{bd} the total charge collected on the gate until breakdown with the gate current. The oxide field at the point of injection depends on the distance from the drain and on V_{gd}, but is smaller than about 0.5 MV/cm, compared to about 10 MV/cm in the case of high field injection. From fig. 1 it is clear that for constant gate-drain voltage

$$Q_{bd} I_g = I_g^2 \, t_{bd} = \text{constant}$$

where t_{bd} is the time until breakdown. For increasing values of V_{gd} injection occurs over a larger area, resulting in larger values of $Q_{bd}I_g$, which is confirmed by the results in fig. 1. By estimating the local current density by model calculations, the influence of the oxide field on breakdown will be discussed. A comparison will also be made with the results obtained by high field injection[1].

1) Wolters, D.R., in "Insulating Films on Semiconductors", M. Schulz and G. Pensl editors (Springer Berlin 1981) p. 180.

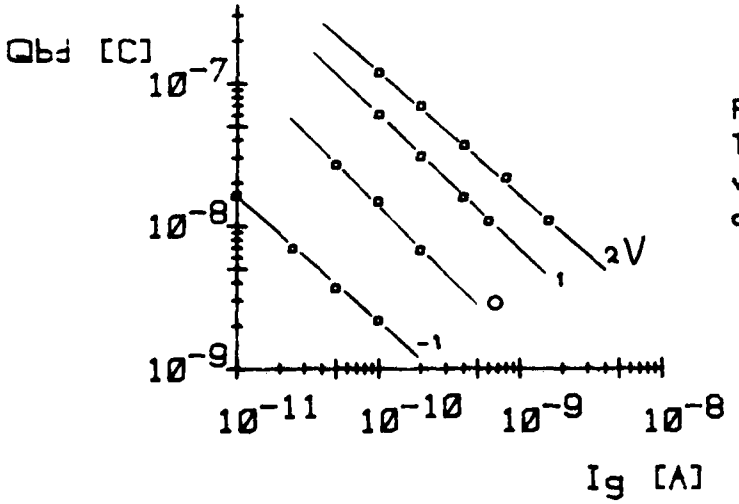

Fig. 1
Total injected charge at breakdown, Q_{bd}, vs gate current, I_g, for several values of the gate drain voltage.

CURRENT INDUCED DIELECTRIC BREAKDOWN

by
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Dielectric breakdown of SiO_2 is investigated with the constant injection current technique to determine whether a current density or an injected charge density is the critical parameter for breakdown. Time to breakdown is measured over a wide range of injection currents. We have compared MOS capacitors with poly-Si and Al gates on thermal oxides with different thicknesses, surrounded by field oxides.
In fig. 1a) time to breakdown is plotted vs. injection current density for poly-Si and Al gates. Straight lines are obtained over many orders of magnitude. However a difference of more than two decades is found between Al and poly-Si. The cumulative charge density Q_{bd}, obtained from fig. 1a is plotted vs. the injection current density in fig. 1b. Generally Q_{bd} is found to be larger for thinner oxides (fig. 2).

The horizontal parts of the curves in fig. 2 suggest a constant Q_{bd}, however a decrease of Q_{bd} is found above a certain current density. The constant value of Q_{bd} fits to the breakdown model of cumulative damage produced by electron injection (1).
A dependence of Q_{bd} on J indicates an increased sensitivity of the oxide breakdown to the current density. A vertical part suggests a critical current density. Examples of constant Q_{bd} and Q_{bd} dependent on J will be shown and discussed.

References. 1. Wolters, D.R., Springer series in Electrophysics **7**, (1981) p. 180.

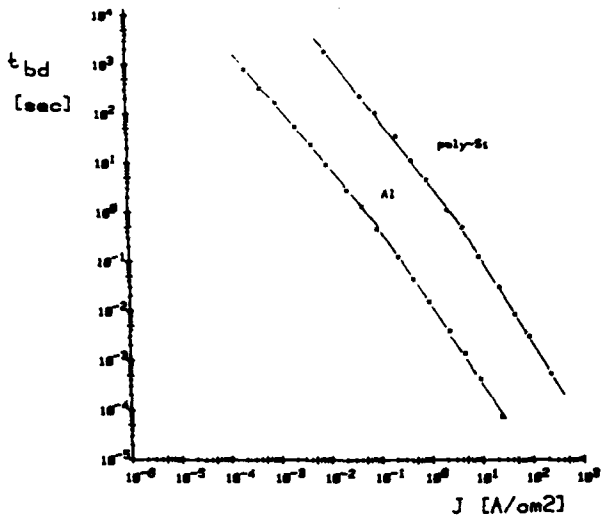

Fig. 1a
Time for breakdown under constant current injection

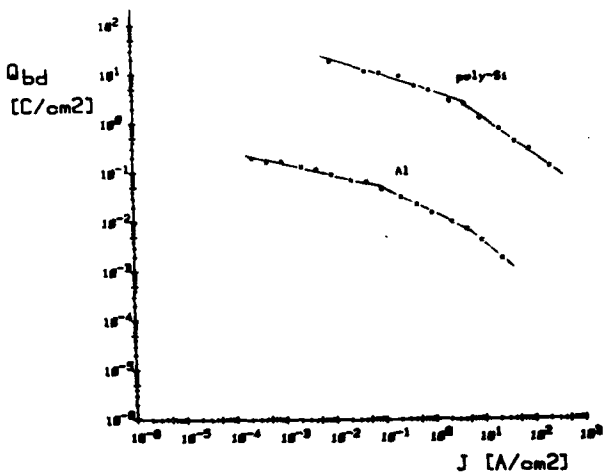

Fig. 1b
Total injected charge density before breakdown under constant current injection

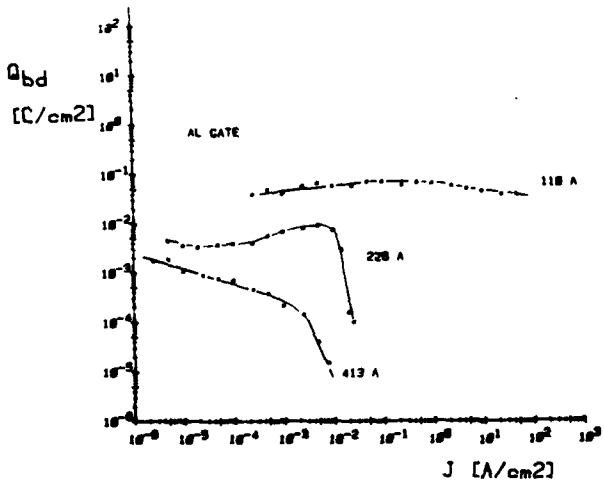

Fig. 2
Total injected charge density before breakdown under constant current injection for different thicknesses of the gate oxides

Charge build-up prior to breakdown in thin MOS gate oxides

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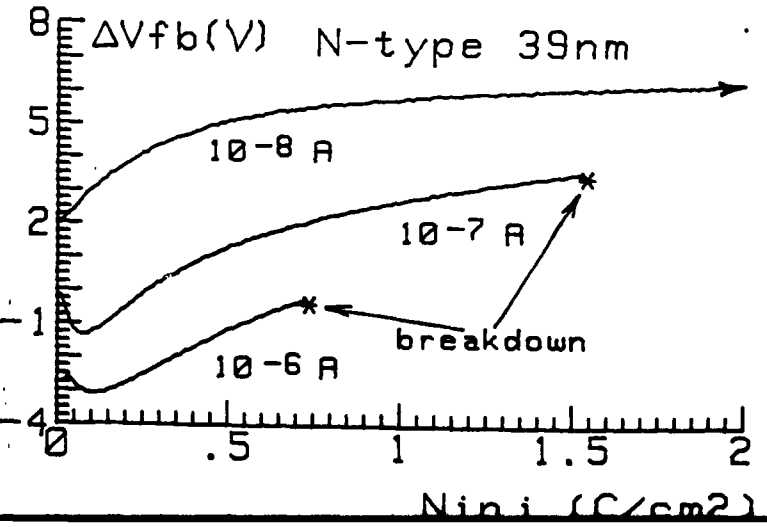
Breakdown phenomena were studied in thin (10-50 nm) thermally grown SiO_2 layers, for use as gate oxides in short-channel MOST technology. Both n- and p-type silicon wafers were oxidized in dry O_2 and chlorine containing O_2 at 900°C. Aluminum gates were deposited using a magnetron sputtering system. Oxides showing no medium field breakdowns and only a very low percentage of low field breakdowns were obtained using optimized processing conditions.

Charge build-up in the oxides was studied using various injection and sensing techniques. Negative charge is detected in the bulk of the SiO_2 layer after voltage stressing in accumulation. Also a build-up of positive charge was found in oxides on both n- and p-type silicon after stresses of either polarity. This charge is located at or near the Si/SiO_2 interface, although some charge near the Al/SiO_2 interface cannot be excluded. It correlates with the so-called "slow states", which have been found in avalanche injection experiments on p-type silicon (1). The amount of positive charge in the oxide is much higher for p-type than for n-type silicon, but the final charge state depends on the sign and the magnitude of the stress voltage.

Taking into account the combined effects of negative bulk and positive interface charge, the shapes of ramp I-V curves measured on n- and p-type samples in accumulation (electrons coming from silicon and aluminum, respectively) can be understood. In n-type MOS capacitors this charge build-up leads to a flat-band voltage shift under constant current injection conditions as depicted in the figure. It is seen that the time-to-breakdown does not depend on the total amount of injected charge, as was suggested previously. Moreover, using one injection condition, it appears that this time is further increased when the slow states are neutralized with a positive gate voltage. The breakdown voltage, as measured with a voltage ramp in accumulation, however, is not affected by the charge state of the slow states.



(1) M. Heyns and R. De Keersmaecker, ESSDERC '81, Toulouse, France, Sept. 14-17, 1981

+ joint Ph. D. study with Middlesex Polytechnic.

++ under grant of State Commitee for Science and technical Progress, Sofia, Bulgaria.

SiO_2 layers on Polycrystalline Silicon

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We investigate the electrical properties of thermally grown SiO_2 films on polycrystalline silicon (poly-Si). These insulating films are used in floating gate memory devices and in poly-Si MOS transistors.
This work is mainly concerned with fine-grained poly-Si (graindiam. typ. 100 ~ 300 nm) but some preliminary results with large-grained poly-Si, obtained with the zone-melting technique [1], will be presented. The construction details of our movable graphite stripheater used for this process, will be presented.
We study the dielectric conduction in the SiO_2 layer grown in a dry O_2 ambient onto poly-Si at 1000° C. It is well-known that the conduction through and breakdown of such oxide layers occur at considerable lower fields than in the case of layers on mono-Si, due to surface roughness [2]. We measure the electric field, E_{ic}, at which a predetermined conduction current is reached as a function of the oxide thickness. The thickness of the oxide layer ranges from 50 to 210 nm. The measurements show that E_{ic} increases with decreasing oxide thickness. This effect was found before with layers thicker than 200 nm [3], and can be explained by a qualitative model. This model is supported by TEM and SEM micrographs which show the morphological aspects of the poly-Si layer and its oxide. We will also present results of measurements on SiO_2 layers grown at 950 and 900° C. We calculate an effective SiO_2/poly-Si barrier height from Fowler-Nordheim plots. This barrier height is used as a parameter for the quality of the SiO_2/poly-Si interface.

[1] B.Y. Tsaur et al - IEEE Electron Dev. Lett. EDL-2, 241 (1981).
[2] R.B. Marcus, T.T. Sheng, P. Lin - J. Electrochem. Soc. 129, 1282 (1982).
[3] D.J. DiMaria, D.R. Kerr - Appl. Phys. Lett. 27, 505 (1975).

AUTHOR INDEX

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